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MARTIN MARIETTA

MARTIN COMPANY

ADVANCED CONTROL SIGNAL PROCESSOR

Phase III Completion Report

Contract No. NAS 8-11684

OR 8722 February 1967

Prepared for

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National Aeronautics and Space Administration
Huntsville, Alabama

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SUMMARY

ELECTRICAL DESIGN

Only minor changes were made on circuits shown in the Pnase I Completion Report with the exception of the comparator which was redesigned for better performance. Final schematic diagrams for all circuits are included.

OVERALL PACKAGE DESIGN

The Phase III prototype ACSP unit consists of 30 encapsulated circuit modules comprised of 114 thin film substrate assemblies. Each of the three channels consists of 10 circuit modules and an inverter output capacitor mounted on a laminated, plug-in channel card. The 33 relays in a system are packaged in three identical, encapsulated, plug-in modules (one for each channel) which are bolted together in a single plug-in assembly.

A wiring harness is used to interconnect the three input-output connectors, the three channel card connectors, and the three relay module connectors.

The ACSP enclosure is a welded aluminum assembly of four machined sides and a machined base. The lid consists of a sheet metal dome formed by the Martin Company Baltimore Division MARFORM process and a machined flange to which the dome is welded.

Elastromeric seals are used throughout the ACSP in the connectors, purge valves, elapsed time counter, and cover.

Discrete components are soldered to pads on small printed circuit cards bonded to the ceramic substrates containing thin film circuits. All connections between thin film substrates and their associated PC cards are made with 0.002 inch diameter gold plated copper wires thermocompression bonded to pads on the substrates and soldered to pads on the PC cards. This technique relieves thin film substrate pads from mechanical stresses by the relatively large discrete component leads. It also facilitates component replacement during assembly and test.

Substrate assemblies are conformally coated with silicone rubber and then assembled into modules along with a PC interconnection card at the base of the module. The module assembly is then encapsulated with a semirigid potting compound.

MICROCIRCUIT FABRICATION

Thin film circuits in the ACSP are made using a subtractive process in which chromel C is vacuum deposited on a glazed ceramic substrate. This is followed by a gold flash, after which the substrate is removed from the vacuum chamber and electroplated with cyanide gold. Selective photoetching is then used to define conductor and resistor patterns.

The thin film resistor values are adjusted to final value by either thermal or mechanical means, and then overcoated with silicon monoxide to prevent further oxidation and provide long term stability. The tolerances on thin film resistor values are either 1 or 5 percent and all resistors have a specified maximum temperature coefficient of resistance of ±50 parts per million per degree centigrade. Conductors have a nominal resistivity of 0.01 to 0.02 ohms per square with 0.03 ohms per square as a specified maximum.

In the latter part of Phase III, it was found necessary to apply a protective sealer coating over the thin film resistors to prevent them from being damaged by contamination such as flux residue.

COMPONENT ATTACHMENT AND INTERCONNECTIONS

Initial attempts to solder components directly to gold pads on thin film substrates led to severe solder-gold amalgamation and joint deterioration during high temperature exposure. Later attempts to solder components to nickel-plated pads on substrates still produced bonds that deteriorated in strength after extended exposure to high temperatures and during temperature cycling.

These problems were overcome by the development of a component attachment method that involved the use of a separate, small printed (circuit) card (with copper pads) to which all discrete components were soldered. The PC card was bonded to the surface of its associated thin film substrate and connections made between the two through "clearance" holes in the PC card with 0.002 inch diameter gold-plated copper wires thermocompression-bonded to pads on the substrate and soldered to pads on the PC card.

TEMPERATURE TESTS

Results of temperature tests taken over a heat sink temperature range of -55°C to +105°C are presented.

EMI TESTS

Results of EMI tests conducted on the prototype, presented in this report, show that in most cases measured noise levels are well within MIL-I-6181D limits with the exception of conducted noise on the output test cables. The measured noise levels would all have been within specifications if the input power cables and monitor leads had been separated from the main cable harness as in the CSP.

LEAKAGE TESTS

Leakage measurements made on the prototype unit with its elastromeric seals indicate a rate of leakage two or three orders of magnitude better than required to meet the required leakage specification.

VIBRATION, SHOCK, AND ACCELERATION TESTS

A description of both preliminary and final vibration analysis and testing is presented. During the period of environmental testing, several modifications were made to the ACSP enclosure, modules, and printed circuit channel cards in order to reduce certain high transmissibility levels. During the final sine and random vibration tests conducted after all modifications had been incorporated, the only failures were modules containing defective components, particularly transistor devices.

No failures of any kind occurred during the shock and acceleration tests.

I. ELECTRICAL DESIGN

Minor schematic modifications were made on several of the schematic diagrams shown in Phase I Completion Report. The final schematic diagrams are shown in Figures 1 through 8. Changes in the majority of schematics were made because of schematic errors and component value or interconnection changes. The only exception is the comparator circuit (Figure 6) which was redesigned for better performance. The temperature results were presented in Phase II Completion Report.

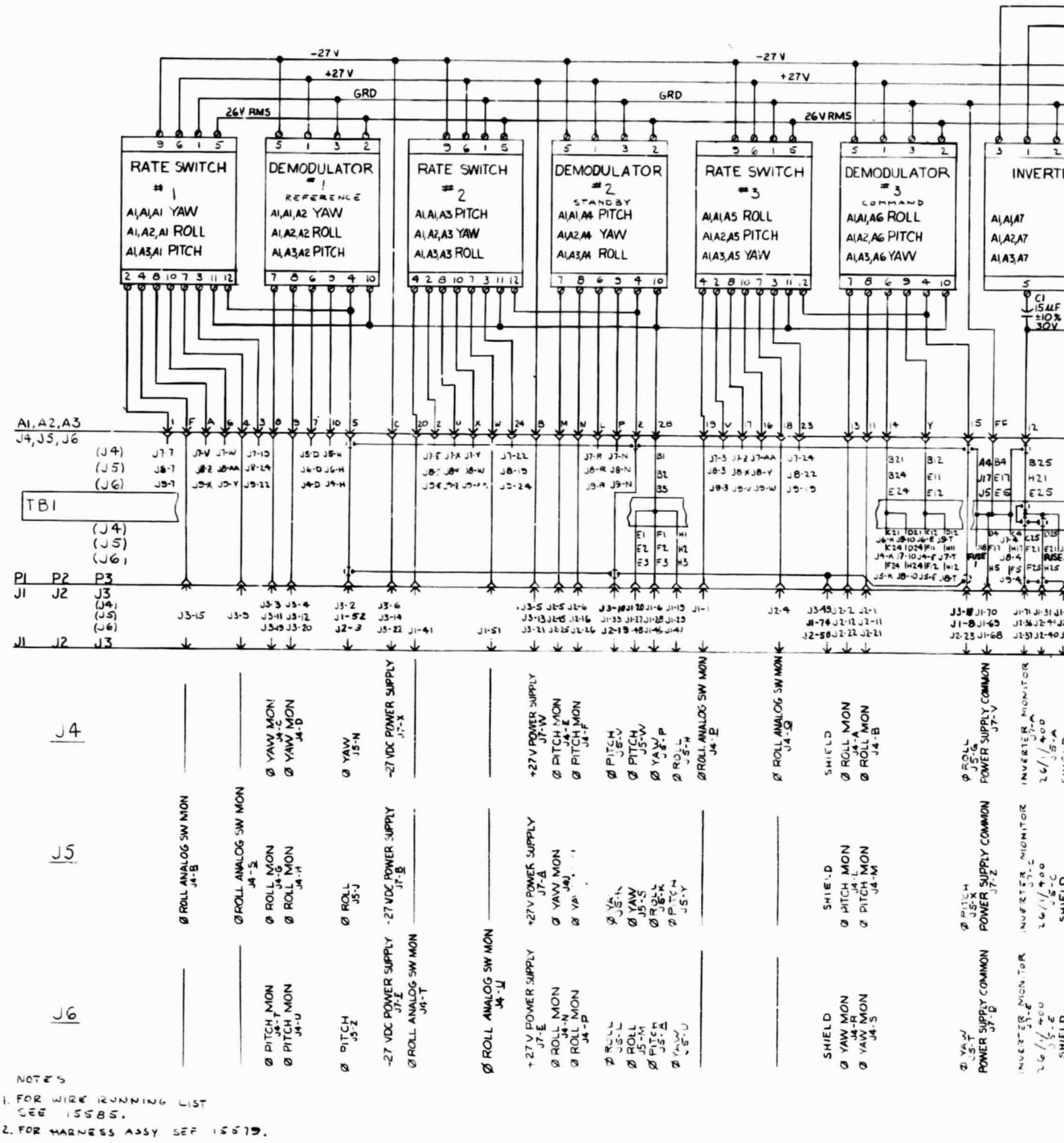
The cables constructed for operation with the ACSP test console were as follows:

1. Test console to prototype

2. Test console to power source (+28 Volts)

3. Test console to wheel speed oscillators.

The test console includes all dummy loads, control potentiometers, switches, and monitor points necessary for operation with the Phase II breadboard or the Phase III prototype.

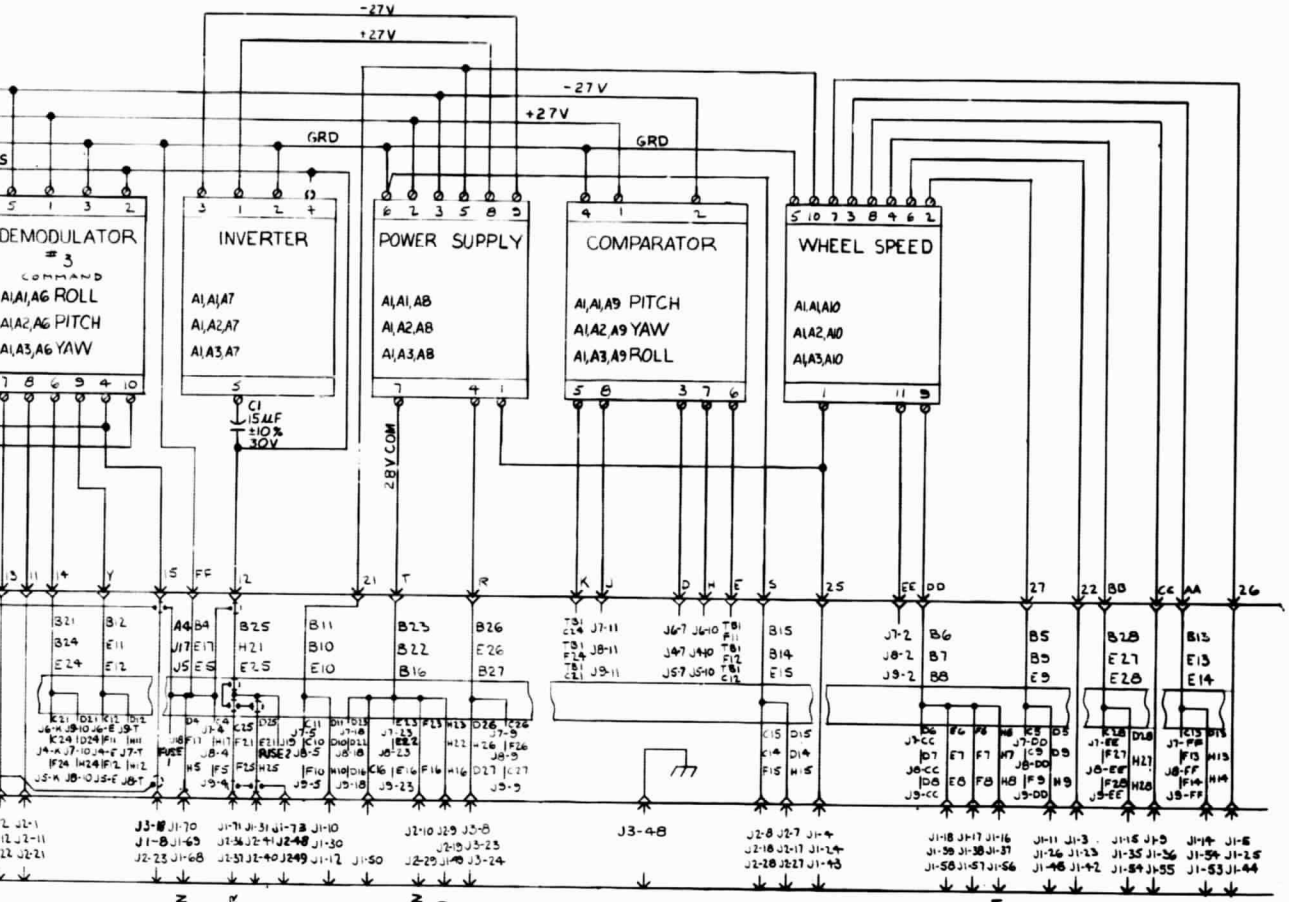


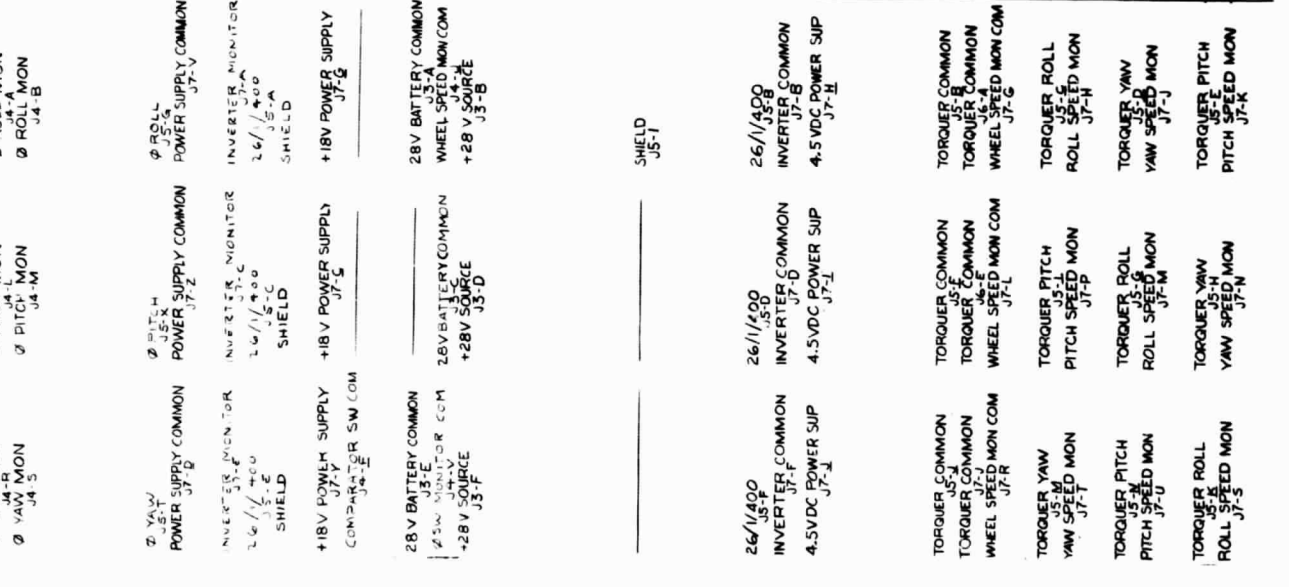
NOTES

1. FOR WIRE RUNNING LIST SEE 15585.
2. FOR HARNESS ASSY SEE 15579.

Figure 1. System Interconnections

FOLDOUT FRAME 1





FOLDOUT FRAME 2

FOLDOUT FRAME 1

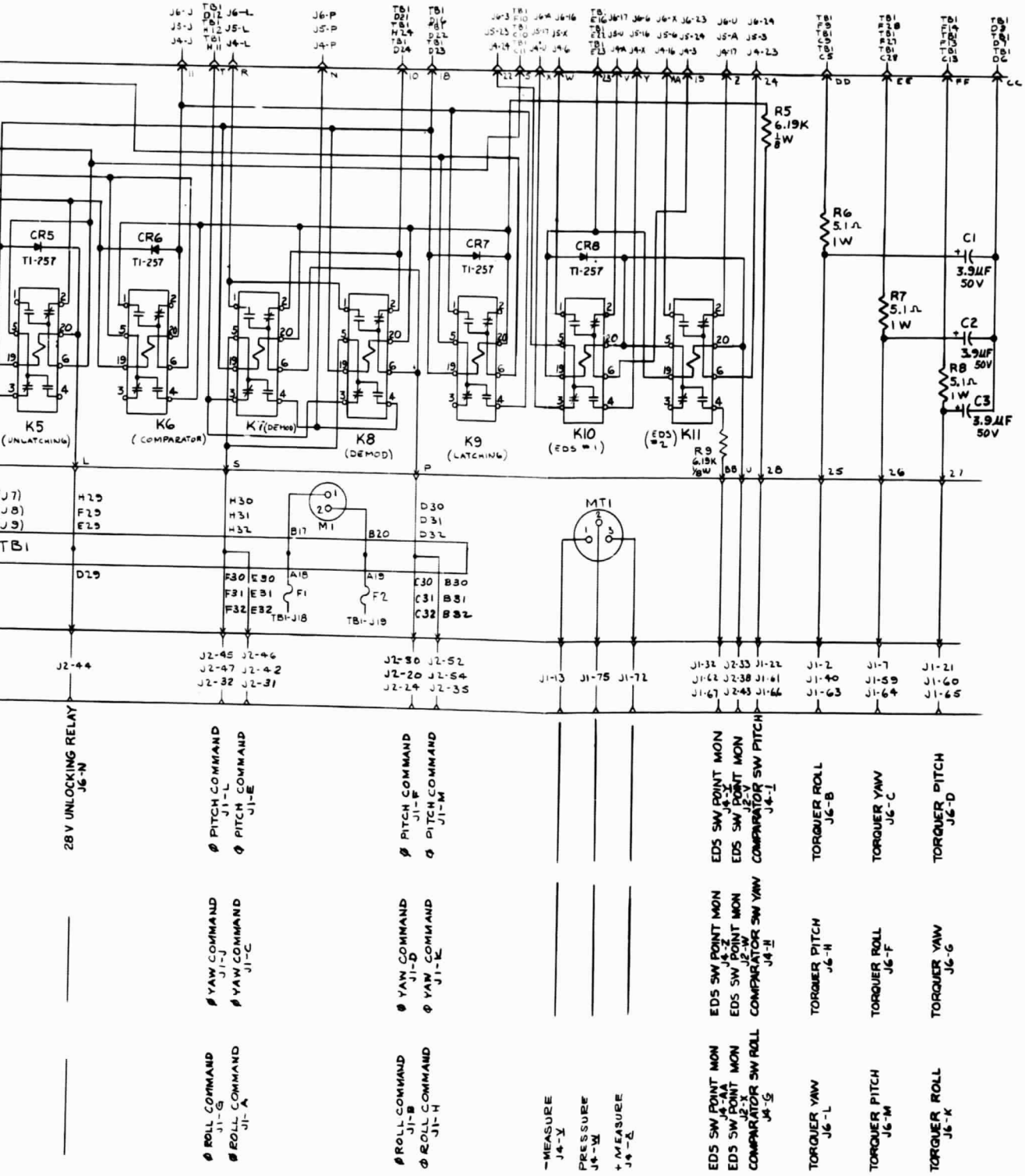
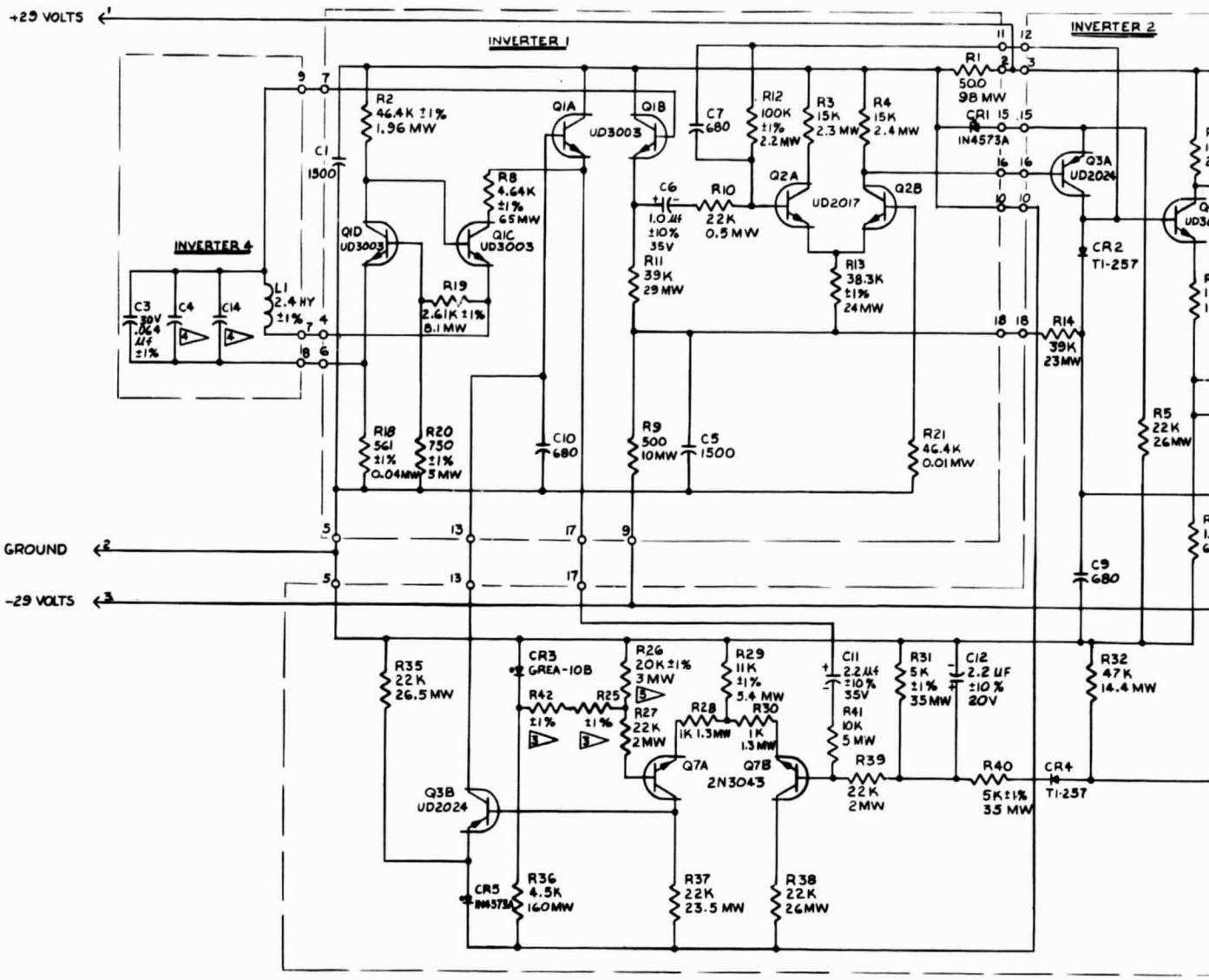
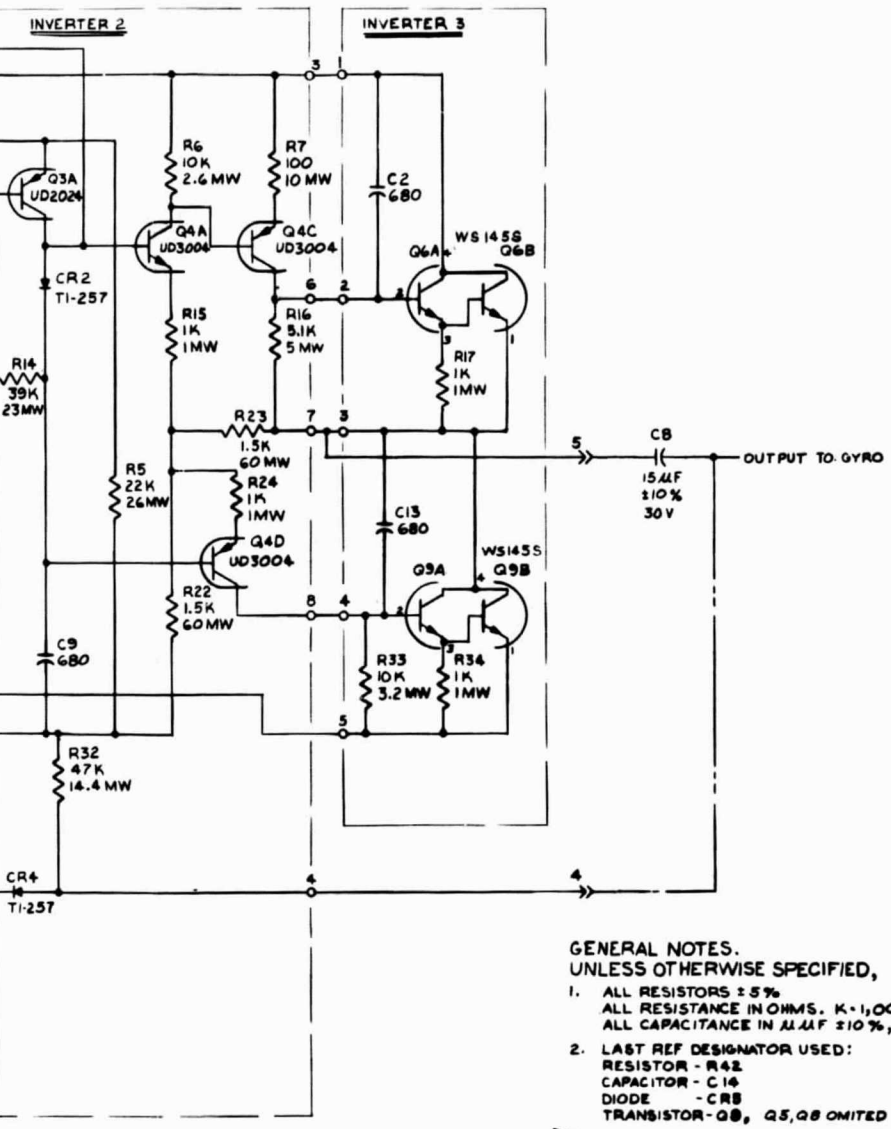


Figure 2. Relay Interconnections

FOLDOUT FRAME 2



FOLDOUT FRAME 1

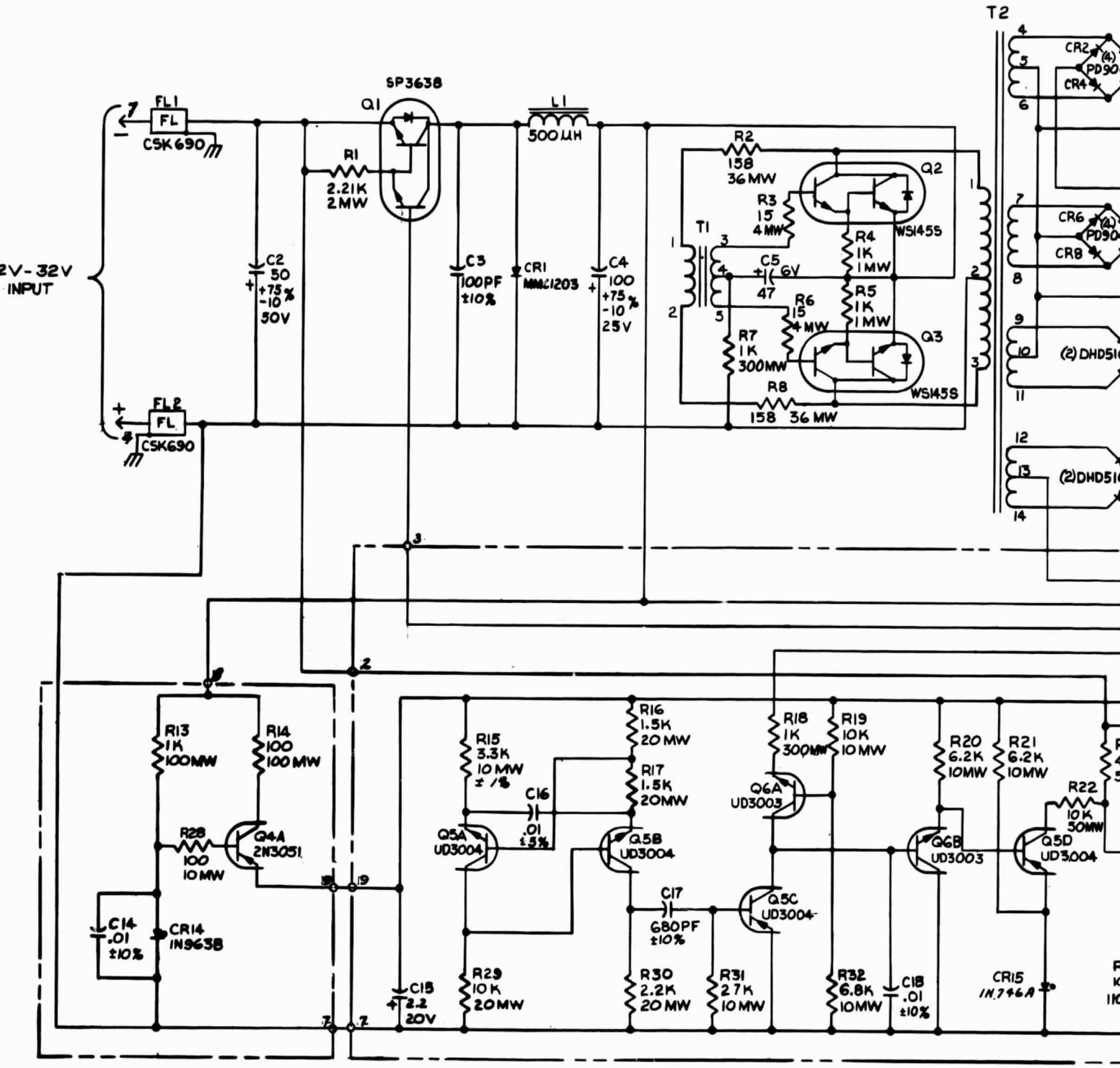


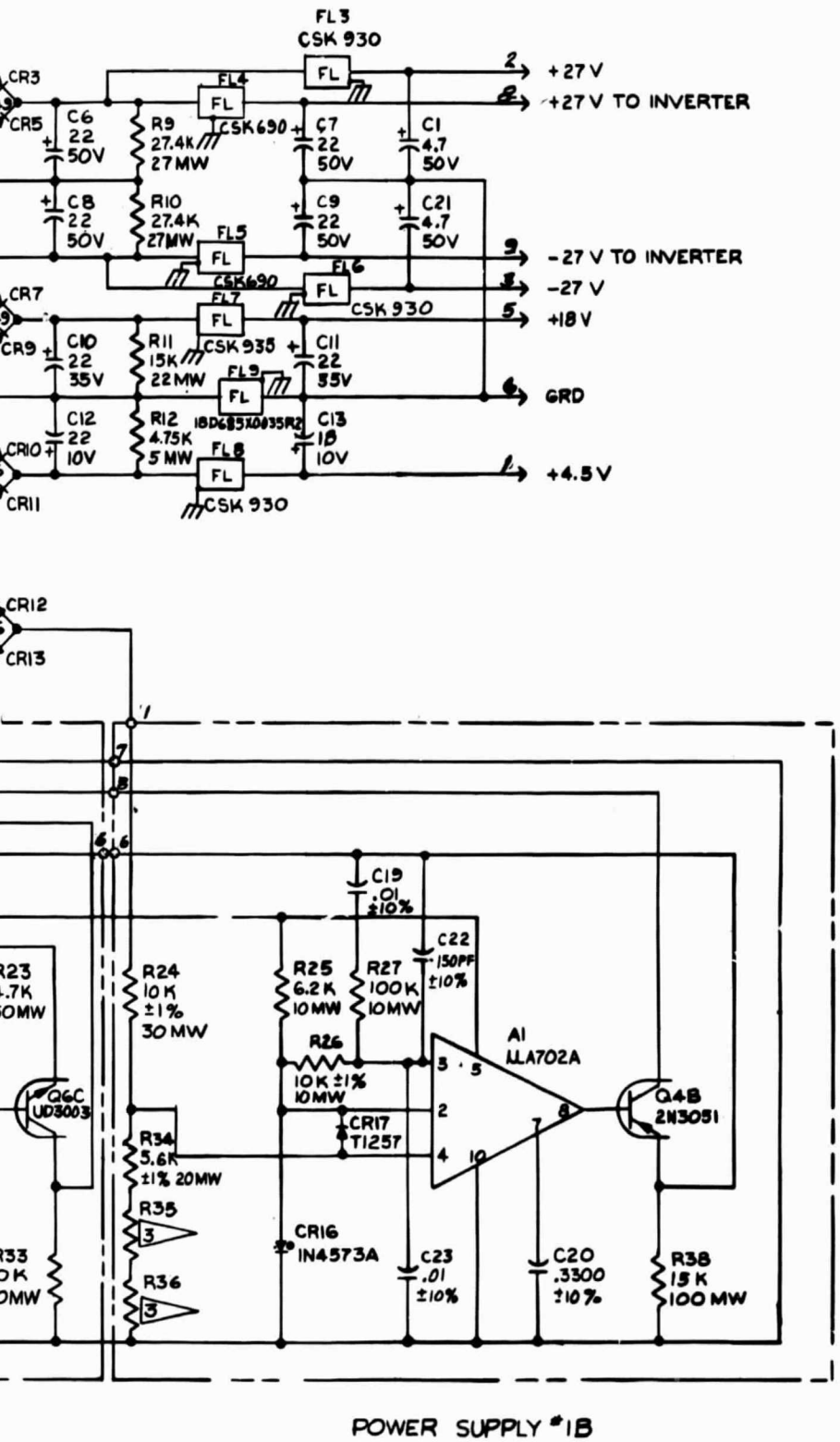
GENERAL NOTES.
UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTORS ±5%
   ALL RESISTANCE IN OHMS. K=1,000 OHMS
   ALL CAPACITANCE IN µµF ±10%, 50 V
2. LAST REF DESIGNATOR USED:
   RESISTOR - R42
   CAPACITOR - C 14
   DIODE - CR8
   TRANSISTOR - Q8, Q5, Q8 OMITED
3. SELECTIVE RESISTOR. VALUE TO BE DETERMINED DURING ASSEMBLY (APPROX VALUE 3.8K 3.8 MW).
4. SELECTIVE CAPACITOR. VALUE TO BE DETERMINED DURING ASSEMBLY. (APPROX VALUE 1500 µµf 100V).
5. R26 SHALL HAVE THE SAME ENVIRONMENTAL CHARACTERISTICS AS R25.
7. MODULE PINS ARE SHOWN AS MALE PINS.

Figure 3. Inverter

FOLDOUT FRAME 2





POWER SUPPLY #1B

GENERAL NOTES:

UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ±5%
   ALL RESISTANCE IN OHMS. K=1000 OHMS
   ALL CAPACITANCE IN µF ±20% 100 V

2. LAST REF DESIGNATOR USED

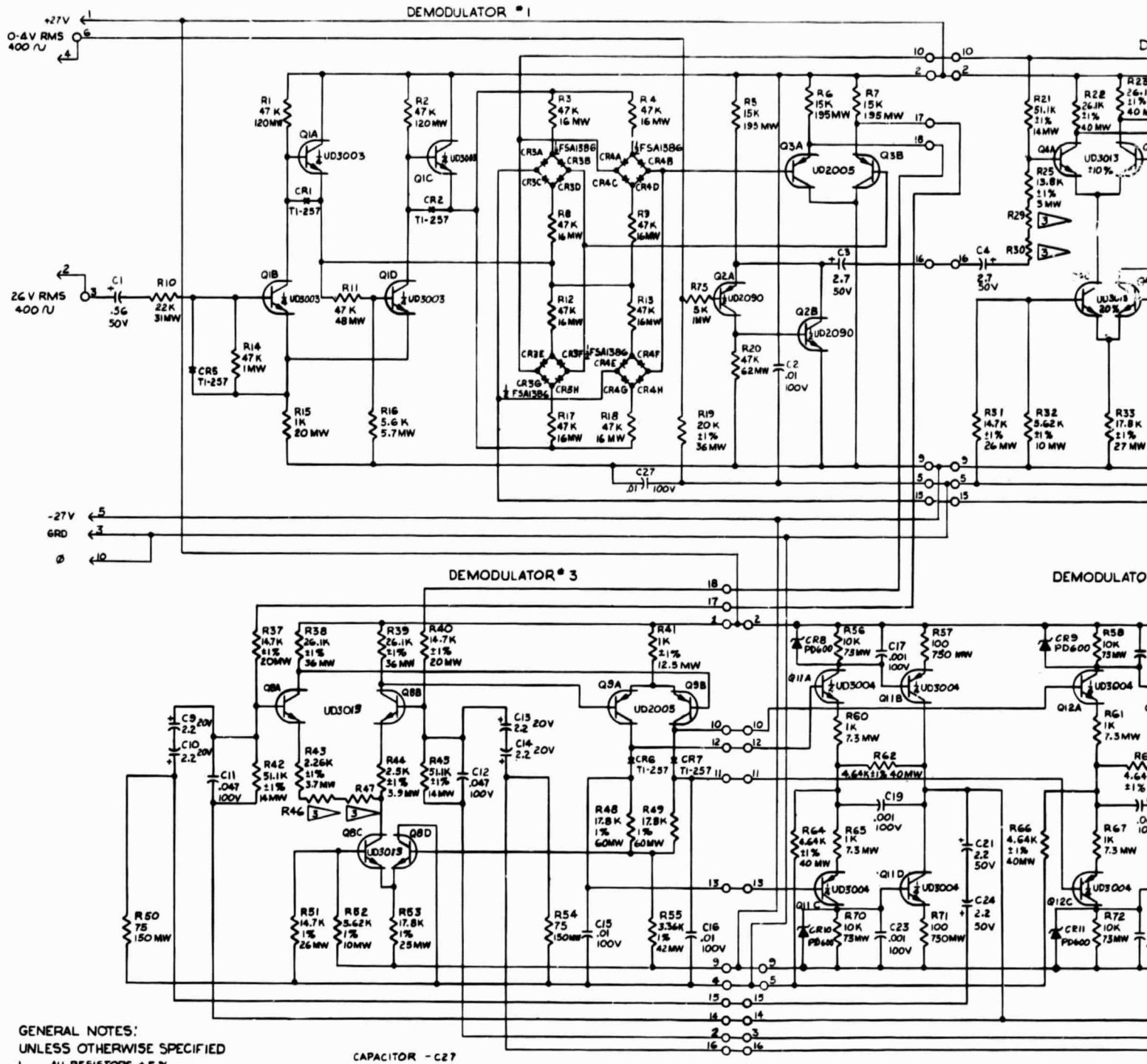
RESISTOR	R38
CAPACITOR	C23
DIODE	CR17
TRANSISTOR	Q6
INDUCTOR	L1
TRANSFORMER	T2
INTEGRATED CIRCUIT	A1
FILTER	FL9

3. SELECTIVE RESISTOR. EXACT VALUE TO BE DETERMINED AT ASSEMBLY.

4. MODULE PINS ARE SHOWN AS MALE PINS

Figure 4. Power Supply

FOLDOUT FRAME 2



GENERAL NOTES:
UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ±5%
   ALL RESISTANCE IN OHMS. K=1,000 OHMS
   ALL CAPACITANCE IN μF ±10%
2. LAST REF DESIGNATOR USED:
   RESISTOR - R77
   CAPACITOR - C27
   DIODE - CR11
   TRANSISTOR-Q12, Q7 & Q10 OMITED
3. SELECTIVE RESISTOR. VALUE TO BE DETERMINED AT ASSEMBLY.
4. MODULE PINS ARE SHOWN AS MALE PINS.

FOLDOUT FRAME 1

FOLDOUT FR

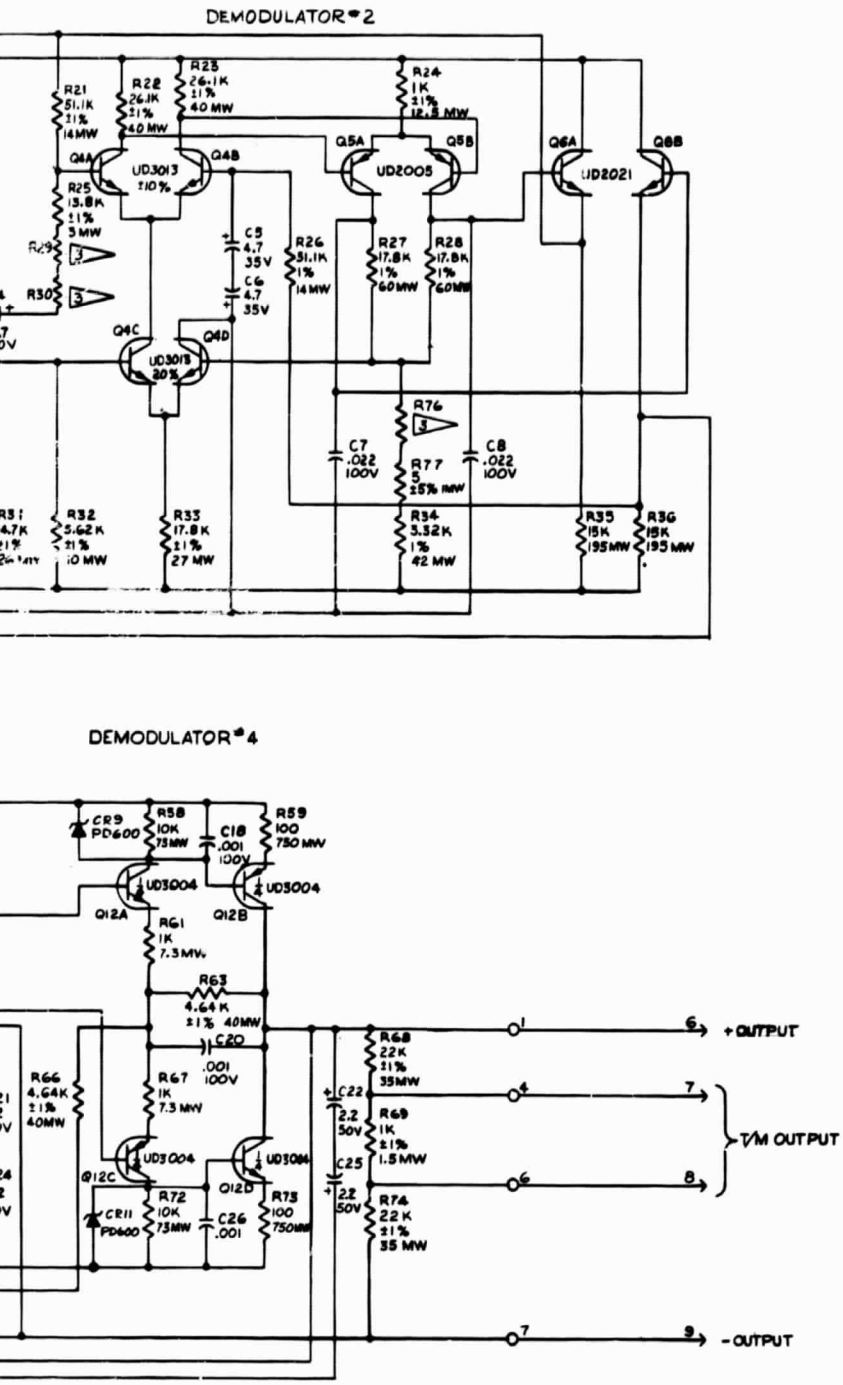
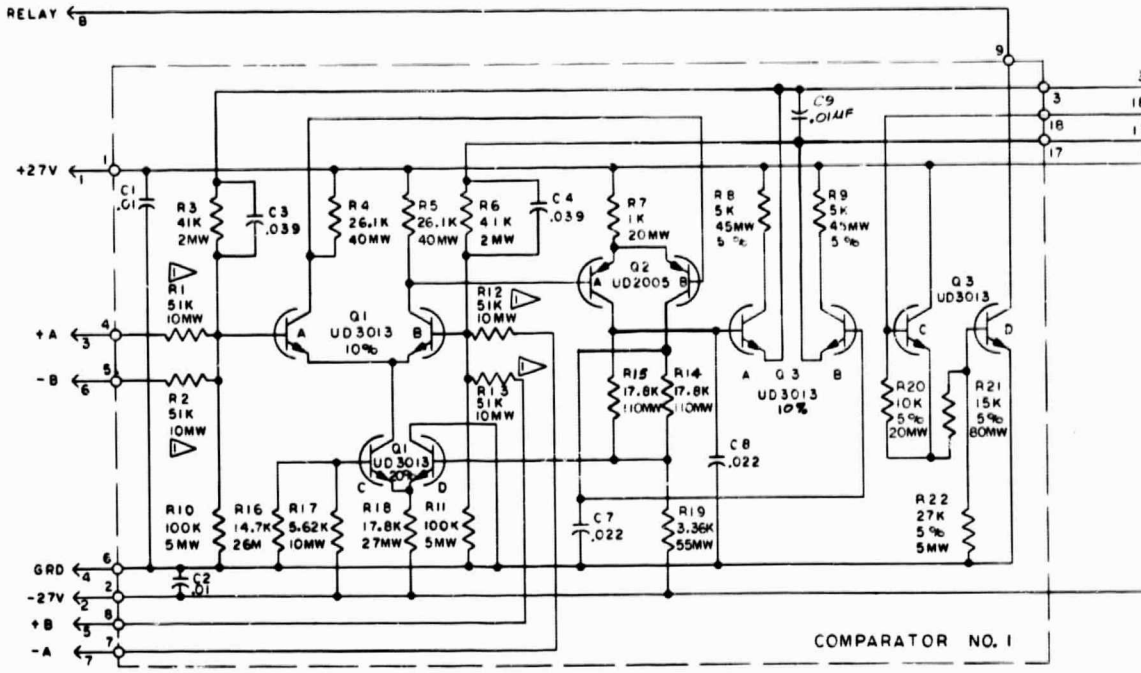


Figure 5. Demodulator

FOLDOUT FRAME 2



GENERAL NOTES:
UNLESS OTHERWISE SPECIFIED

1. RESISTANCE IN OHMS, K=1000
   RESISTORS ± 1%
   CAPACITANCE IN MICROFARADS
   CAPACITORS ± 10%, 100V

2. LAST REFERENCE DESIGNATOR USED:

RESISTOR	R44
CAPACITOR	C9
DIODE	CR4
TRANSISTOR	Q6

(1) 3. R1 AND R2 TO BE WITHIN 50 OHMS OF EACH OTHER.
R12 AND R13 TO BE WITHIN 50 OHMS OF EACH OTHER.

4. MODULE PINS ARE SHOWN AS MALE PINS.

(2) 5. RESISTOR VALUE TO BE SELECTED AT ASSEMBLY FROM ASSORTMENT SHOWN ON PARTS LIST.

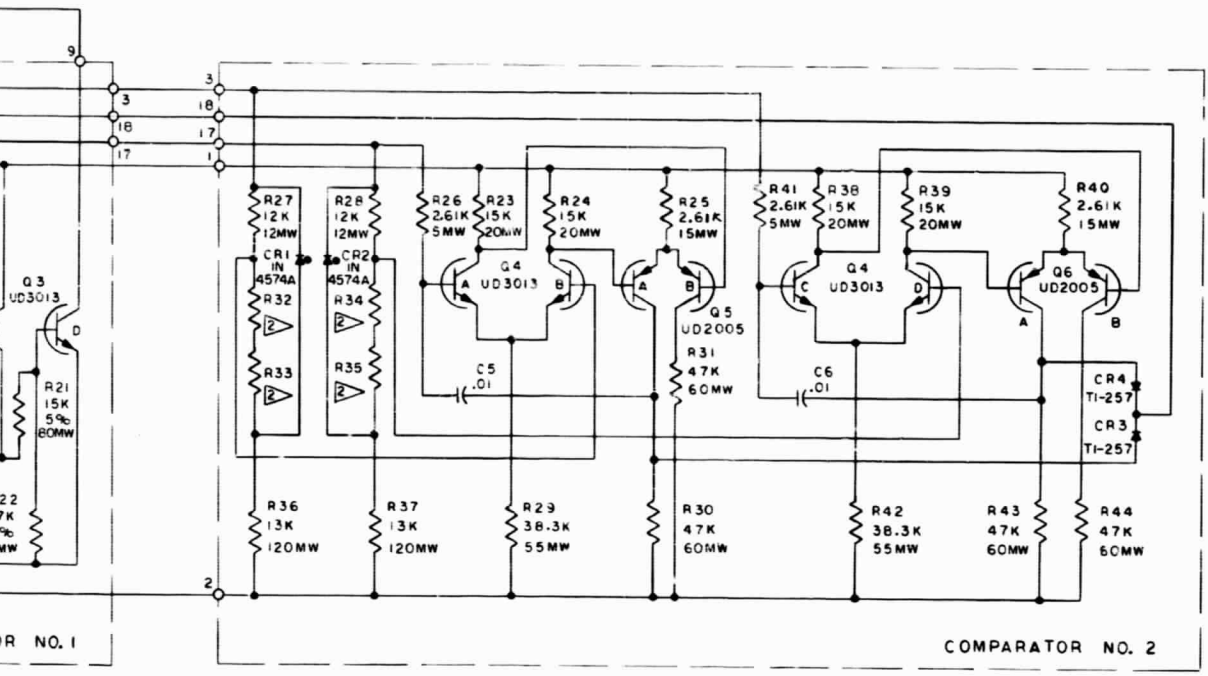
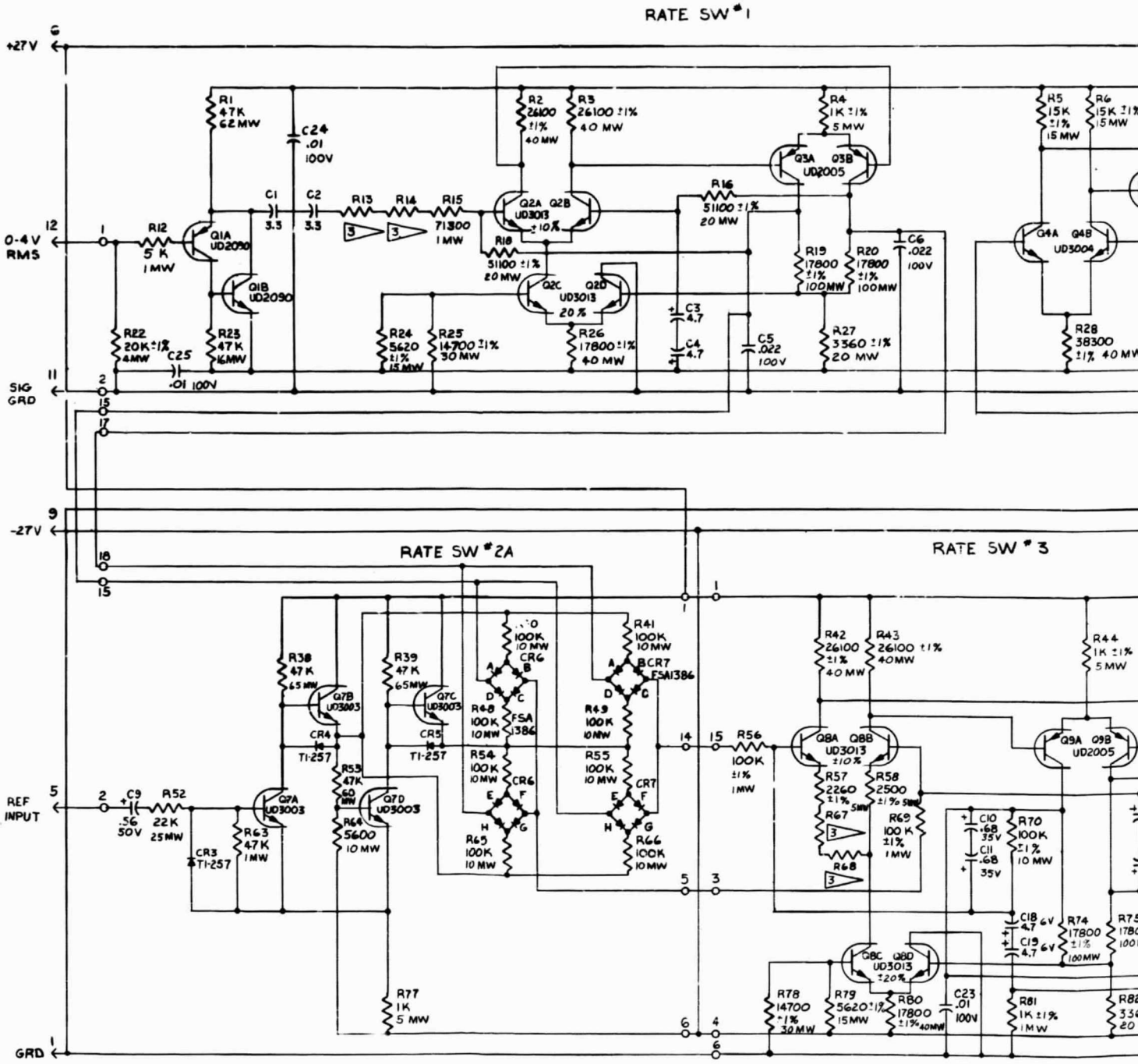


Figure 6. Comparator

FOLDOUT FRAME 2



GENERAL NOTES:
UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ±5%
   ALL RESISTANCE IN OHMS. K=1000 OHMS
   ALL CAPACITANCE IN MF ±10% 10V

2. LAST REF DESIGNATOR USED:

RESISTOR	R84
CAPACITOR	C26
DIODE	CR9
TRANSISTOR	Q10

3. SELECTIVE RESISTOR. EXACT VALUE TO BE DETERMINED AT ASSEMBLY.

4. MODULE PINS ARE SHOWN AS MALE PINS

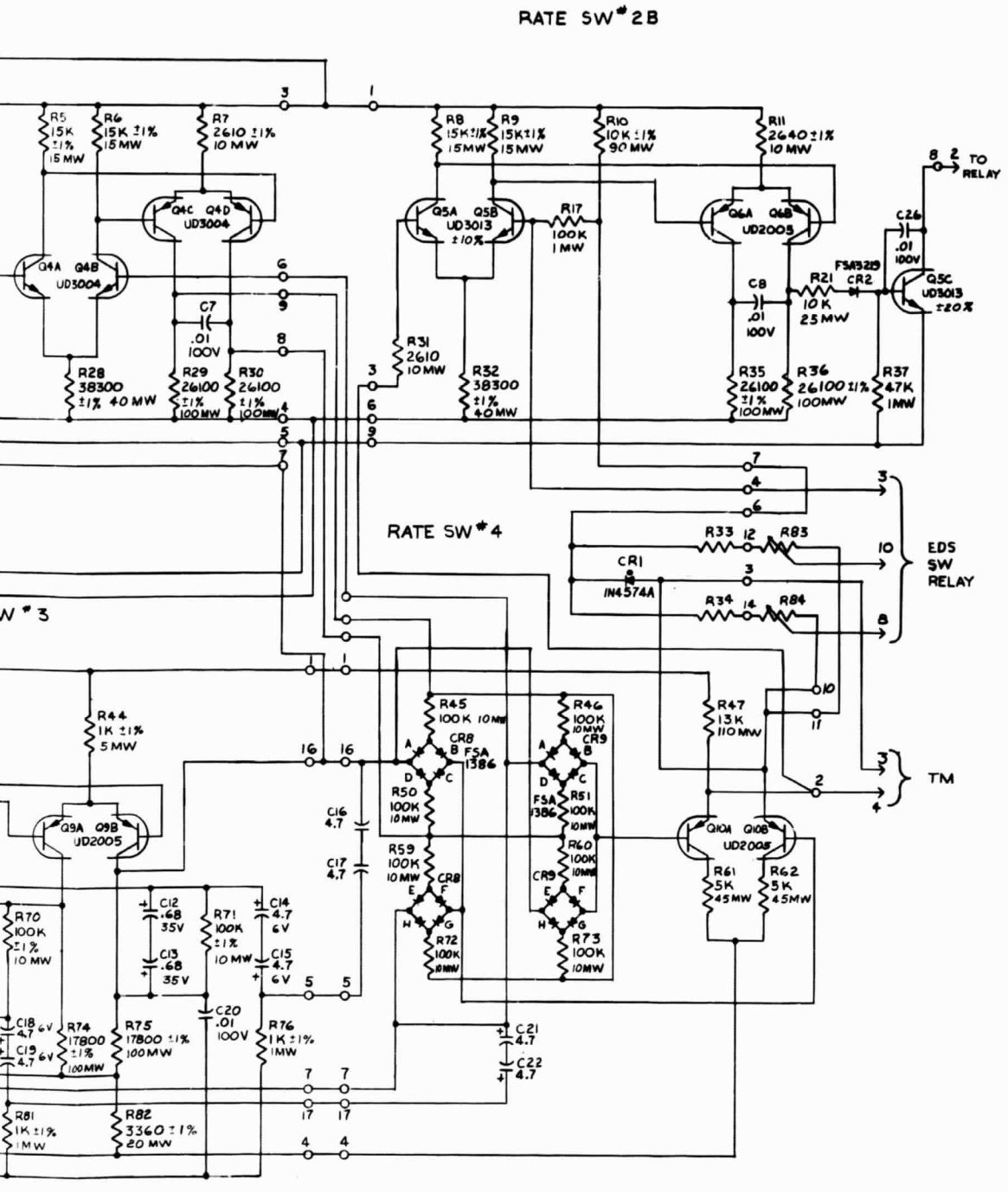
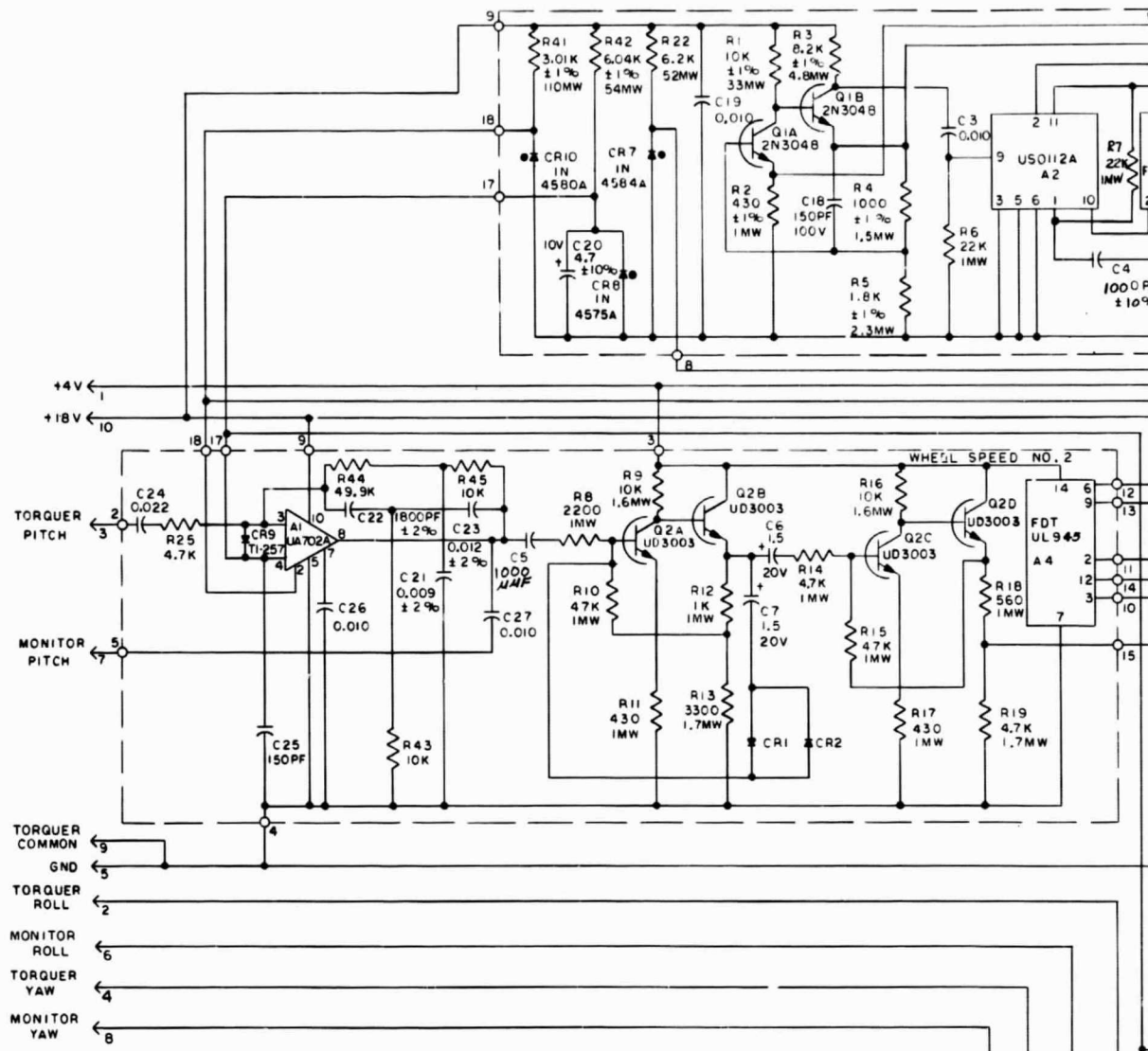


Figure 7. Rate Switch

FOLDOUT FRAME 2



NOTES

1 - ALL RESISTORS ARE IN OHMS AND ± 5% UNLESS OTHERWISE NOTED.

2 - ALL CAPACITORS ARE IN UF, 100V & ± 10% UNLESS OTHERWISE NOTED.

3 - ALL DIODES ARE TI-257 UNLESS OTHERWISE NOTED.

(1) 4 - SELECT R28 FROM VALUES LISTED ON PARTS LIST AT ASSEMBLY.

(2) 5 - SELECT C2 FROM VALUES LISTED ON PARTS LIST AT ASSEMBLY.

6 - LAST COIL L1

7 - LAST RESISTOR R45

8 - LAST CAPACITOR C27

9 - LAST DIODE CR10

10 - LAST TRANSISTOR Q5

11 - LAST INTEGRATED CIRCUIT A7

FOLDOUT FRAME

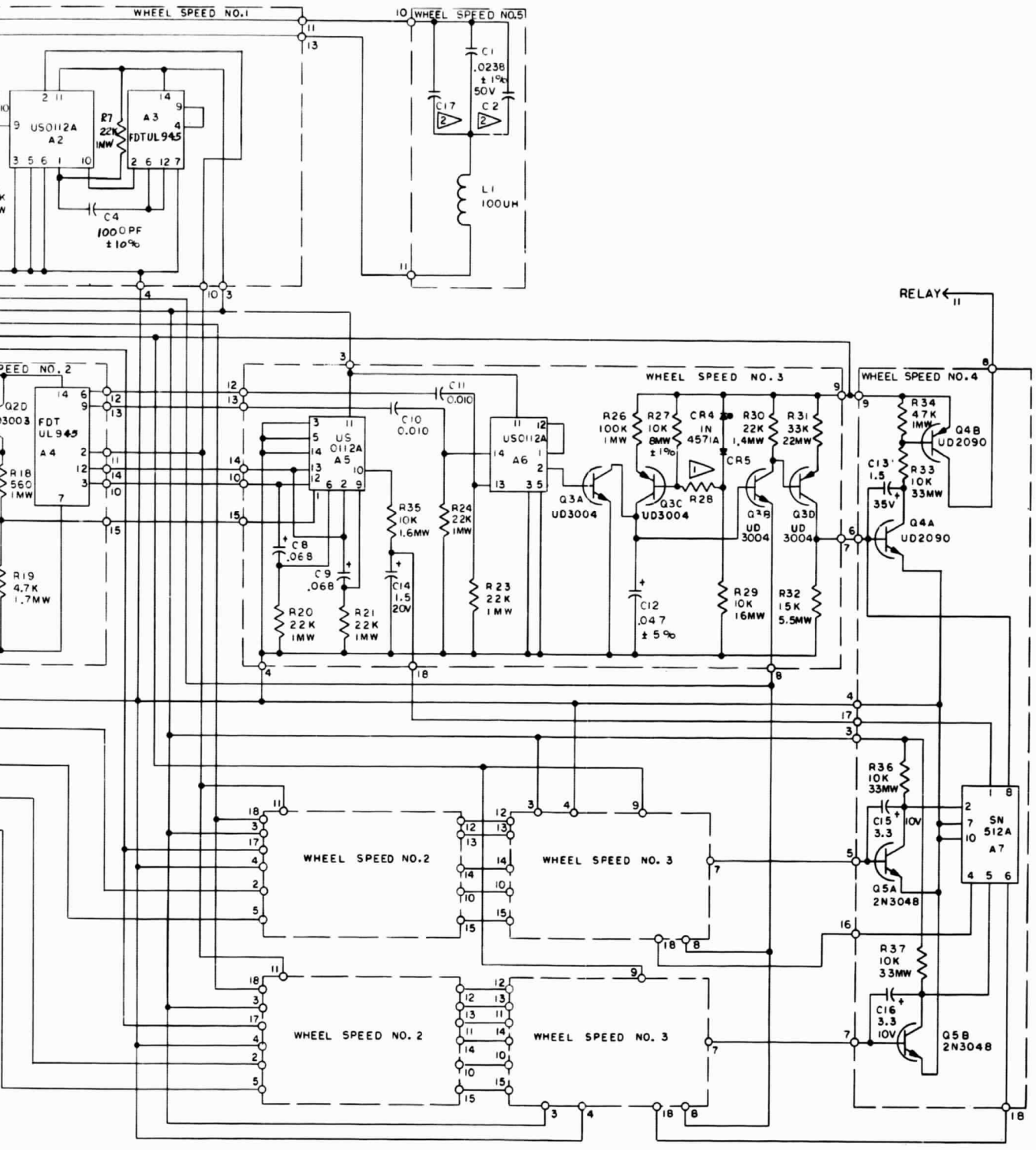


Figure 8. Wheel Speed Sensor

FOLDOUT FRAME 2

II. PACKAGING AND MECHANICAL DESIGN

A. OVERALL PACKAGE CONCEPT

The 30 encapsulated modules of six different circuit types in an ACSP system are comprised of 114 thin film substrates. The modules have input-output pins that are plugged into individual pin sockets on a printed circuit card.

The 30 circuit modules are divided into three interchangeable processor channels of 10 modules each. The 10 modules and one inverter capacitor plug into the printed circuit channel interconnection card (Figure 9) which, in turn, plugs into edge card connectors at the bottom of the enclosure. The interconnection card is a combination of epoxy G-10 and melamine bonded together for structural reasons with Armstrong epoxy X-81 to reduce warping and flexing due to heat and vibration. The modules and channel card are held rigidly in a machined casting (Figure 10) that is attached to the sides of the enclosure. This casting also provides a thermal conduction path to the cold plate.

The 33 switching relays per system are divided into three groups, each of which is associated with one of the processor channels. Eleven relays and 20 discrete components are soldered to a PC card (Figure 11), which also has PC contact fingers at the bottom for insertion into an edge card connector. Each relay has a thin spacer made of G-10 placed between the relay and PC card to avoid shorting the case of the relay to the foil and also to stress on solder joints when clamped together. The assembly is placed in a mold with a stiffening bracket to keep the PC card flat and with five inserts to relieve mounting pressure. They are then encapsulated to finished modules (approximately 5.6 by 1.9 by 0.6 inch each) which are stack mounted on a machined casting. The castings used for mounting the relay modules and processor modules are identical, but are machined differently for the configurations (Figure 12). The processor module casting was revised during vibration tests by the addition of full length PC card supports which increased rigidity and decreased transmissibility.

Since the three input-output connectors require discrete wires that are crimped into individual contacts, it was decided to continue this wiring on

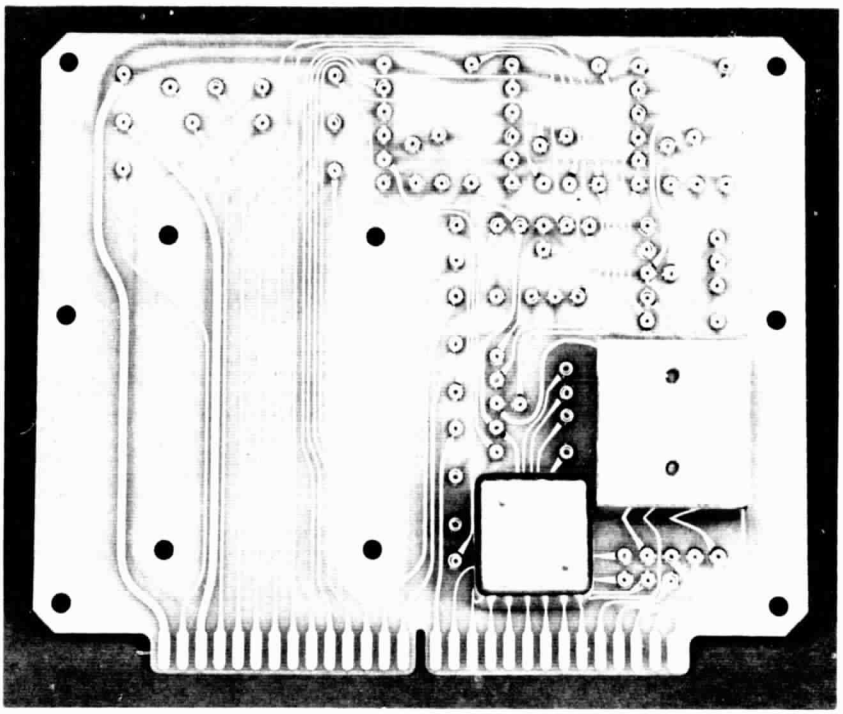


Figure 9. Printed Circuit Channel Interconnection Card

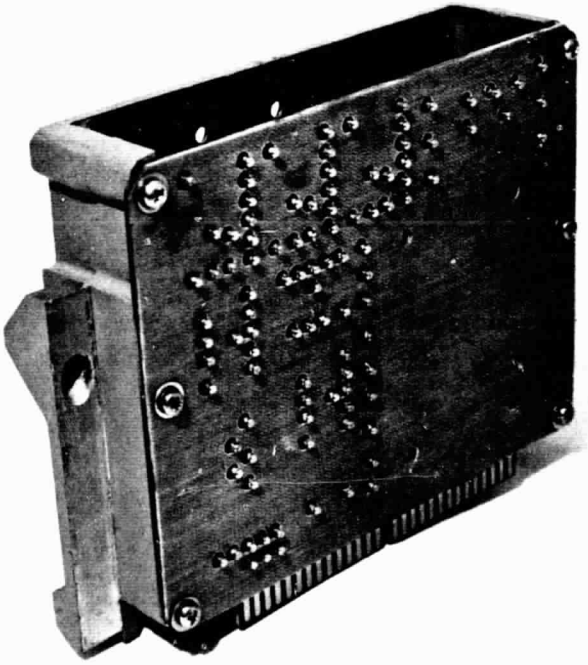
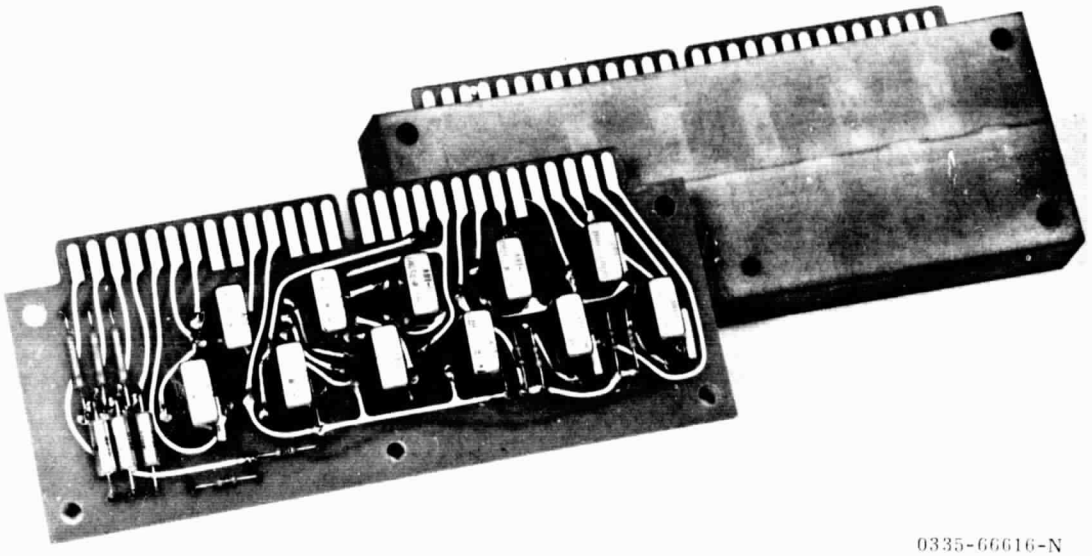


Figure 10. Machined Casting for Holding Modules and Channel Cards



0335-66616-N

Figure 11. Relay Module Before and After Encapsulation

Figure 12. Machined Casting for Holding Relay and Processor Modules

a point-to-point basis rather than terminating the wires near the edge of a board and running printed circuits to the relay and channel connectors. This results in fewer total connections and also allows the use of floating connectors for the relay and channel assemblies. All wiring, including the internal mating portion of the three input-output connectors, the three relay connectors, the three channel connectors, the elapsed time counter, and the pressure transducer are wired and laced outside the enclosure. Service to the wiring assembly would be done outside the enclosure if required.

The enclosure is a welded assembly of four machined sides and a machined base (Figure 13). The sides that contain the vertical mounting and heat transfer columns are machined from 6061-T6 aluminum plate using tape-controlled milling machines. At the bottom of the columns, a taper is machined into the slot that receives the channel frame. The channel frame itself, having a matching taper, is driven against the mounting columns by virtue of the taper and the angled mounting screws. The enclosure base is fabricated in the same manner. The ends are also machined, but are not tape-controlled because of the simplicity of the machining operations.

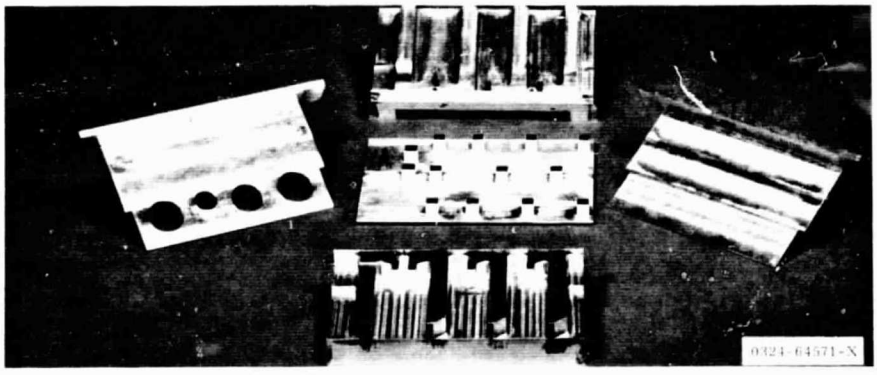
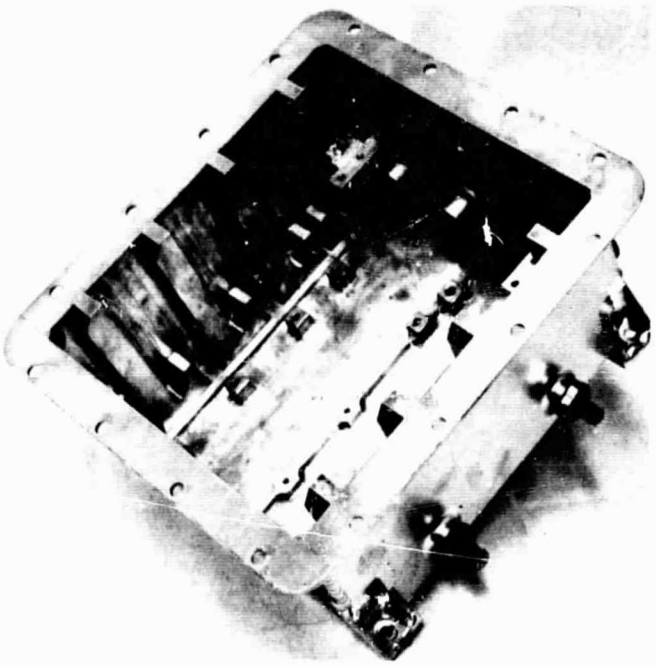


Figure 13. Enclosure Sides and Base

The base and top lips of the four sides are machined thicker than necessary by 0.062 inch to allow for finish machining after welding. The five pieces are held rigidly in a fixture while the four corners are being seam welded around the periphery of the base and at the junction of the four lips (Figure 14). During vibration tests an additional gusset was added to each mounting flange in order to reduce transmissibility.

The enclosure lid assembly is a combination of a formed, sheet-metal dome and machined lip which are welded together (Figure 15). The sheet-metal dome is formed from 6061-T6 aluminum 0.062 inch thick. This was done at the Baltimore Division using the MARFORM process. As in the enclosure, the lip is machined thicker by 0.062 inch than the finished dimension to allow for maching after welding to the dome.

Figure 14. Welded Enclosure



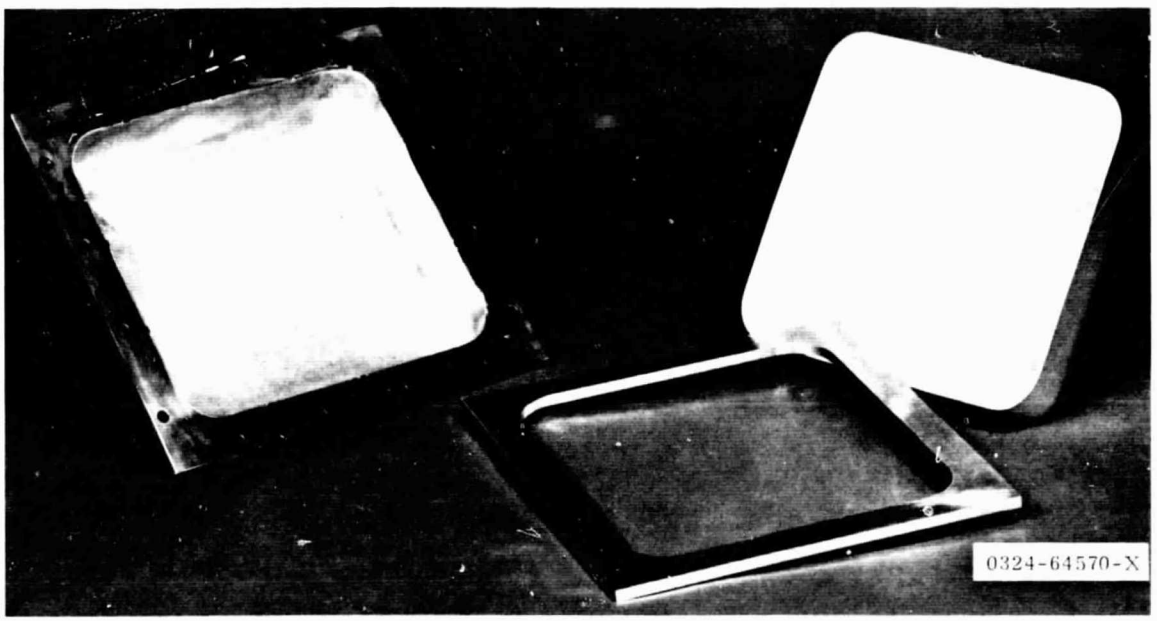


Figure 15. Enclosure Lid Before and After Welding

Sealing of the ACSP to meet the pressurization and leak rate specifications was accomplished using elastomeric seals. The main seal between the enclosure and lid is a Parker Seal Company Gask-O-Seal (Figure 16). It is essentially a machined aluminum spacer (0.1 inch thick) that has grooves machined all the way around on both top and bottom faces. The

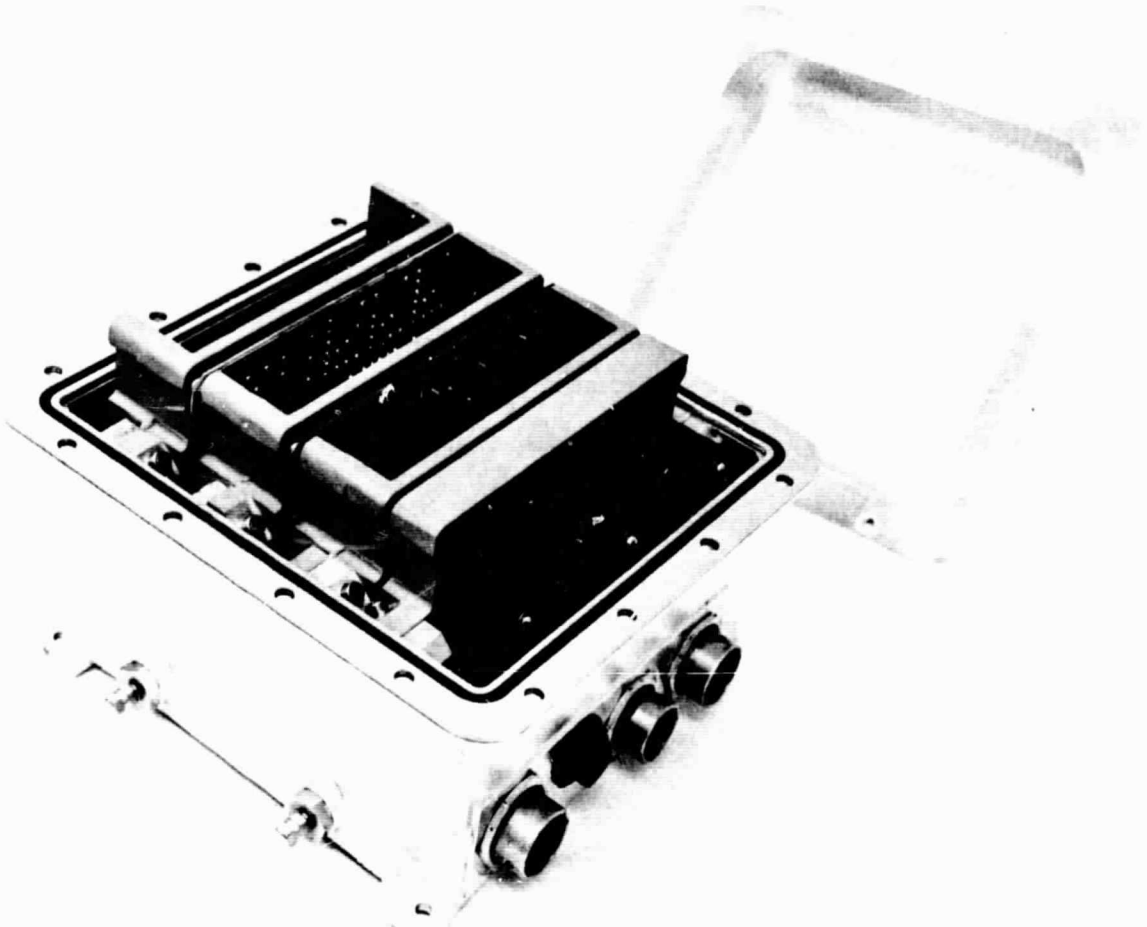


Figure 16. Elastomeric Seal Between Enclosure and Lid

elastomeric compound (VITON) is precision molded into these grooves so that when the 16 rim bolts are tightened to 50 in-lbs each to the point of metal-to-metal contact, the molded compound is displaced into its own groove. This produces an effective seal between the enclosure and its lid. The Gask-O-Seal occupies approximately 34 inches of the total seal length of 54 inches. The remaining seals are associated with the three input-output connectors, the elapsed time counter, and the two purge valves (Figure 16). These components are sealed using VITON O-rings in a conventional compression seal. It should be pointed out that VITON was chosen as the sealing elastomeric because of its low diffusion rate when exposed to elevated temperatures and its low compression set characteristics at low temperatures. Lid and groove finishes required for the Gask-O-Seal and VITON O-rings are 32 to 64 microinches.

A complete ACSP enclosure (Figure 17) was fabricated and successfully proof tested to 30 psig as contractually required. Some characteristics of the ACSP are:

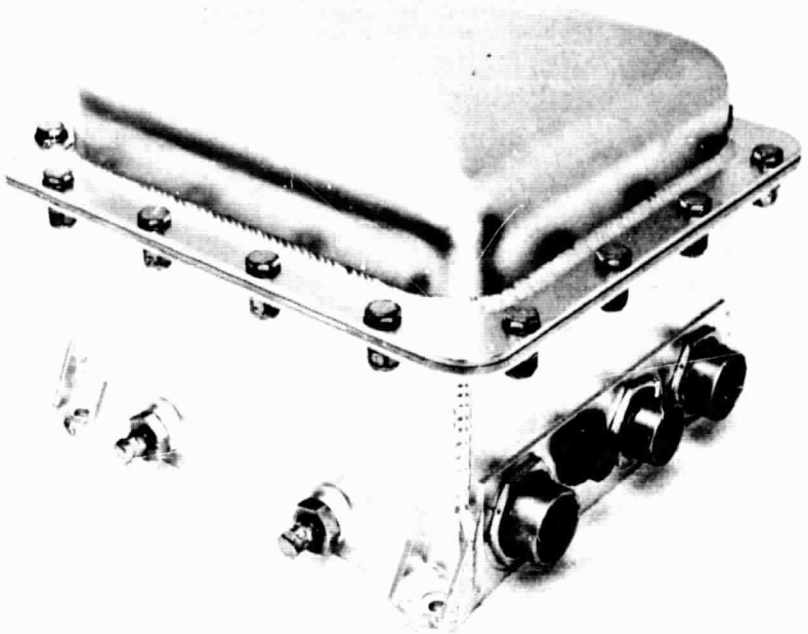


Figure 17. ACSP Enclosure

1. Weight - 21 pounds
2. Internal volume - 430 in^3 (calculated)
3. Packaging density - 23,300 components per ft^3
4. Power dissipation on cold plate - 0.925 watts per in^2
5. Power dissipation - 62 watts (nominal).

B. MODULE DESIGN

The ceramic substrates (1.000 by 1.000 by 0.030 inch) with deposited thin film resistors, conductors, and bonding pads are combined with PC cards (1.000 by 1.000 by 0.010 inch) on which are mounted all discrete components. The card is positioned directly above the ceramic substrate with a separation of 0.010 inch. The purpose of this gap is to allow room on the substrate for 1 mil gold wires for connecting spare resistor segments and to help minimize any stresses applied to the component card or substrate during encapsulation or subsequent thermal and dynamic cycling. During the initial assembly process, this gap is maintained by introduction of a thixotropic epoxy compound through several 0.050 inch diameter holes in the discrete component card.

Electrical connections between the substrate and component card are made by first soldering 0.002 inch diameter gold plated copper wires to copper pads on the component card and then thermocompression bonding the opposite ends to the appropriate pads on the thin film substrate. The latter bond is made through 0.036 inch diameter holes in the component card. A small service loop or slack is introduced between the bonds of the 0.002 inch wire so that any movement or flexing of the component card relative to the substrate will not stress the wire or bonds. The discrete components and wires used to interconnect substrates are soldered to copper pads on component cards. After soldering the other ends of the substrate interconnection wires to a substrate test board (Figure 18), electrical tests are made.

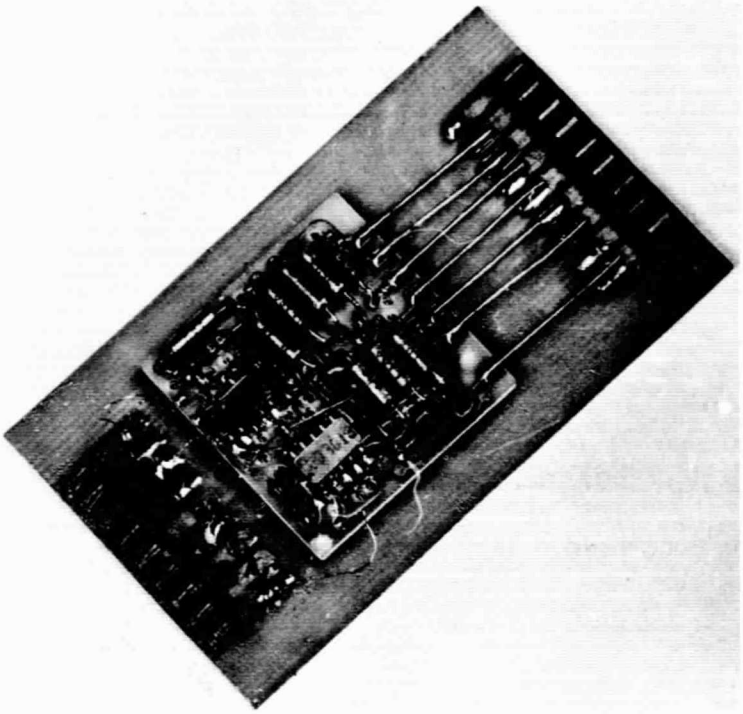


Figure 18. Substrate Interconnection Wires Soldered to Substrate Test Board

All testing of substrates prior to module assembly is done with the substrate assemblies mounted to test boards to eliminate handling of the assemblies. After completion of tests, the 0.010 inch space between the substrate and its associated component PC card is filled with Dow Corning RTV-503 silicone rubber. All components and joints on the PC card are also conformally coated with RTV-503.

Attachment to a 0.032 inch thick PC interconnection card located perpendicular to the substrates at the base of each module is the next assembly step. This PC card also contains the module input-output pins and,

in the case of the inverter, power supply and wheel speed sensor modules, supports PC cards containing relatively large discrete components such as chokes and transformers. The number of substrates per module varies from two to eight. The substrate assemblies are interconnected at the top by cross wire welding to wires previously soldered to pads on the component PC card. In the case of the inverter module (Figure 19), the power transistors and associated components are located on another PC card which is screwed to the heat sink and mounting bracket. Leads from the power stage are brought down to the previously described PC interconnection card. The inside of the heat sink bracket is spotfaced smooth to a 32 microinch finish and Wakefield Thermal Joint Compound No. 120 is applied to this surface before the power stage PC card is screwed in placed The remainder of the modules, with the exception of the power supply, have heat sink and mounting brackets, but do not use power transistors. The module subassembly is again tested electrically and then encapsulated. The heat sink bracket is coated with mold release and screwed to the encapsulation fixture. Input-output pins are plugged into one side of the fixture which has teflon inserts in the pin holes. Encapsulation with Minnesota Mining and Manufacturing CRP 241 compound and a final electrical check complete the module.

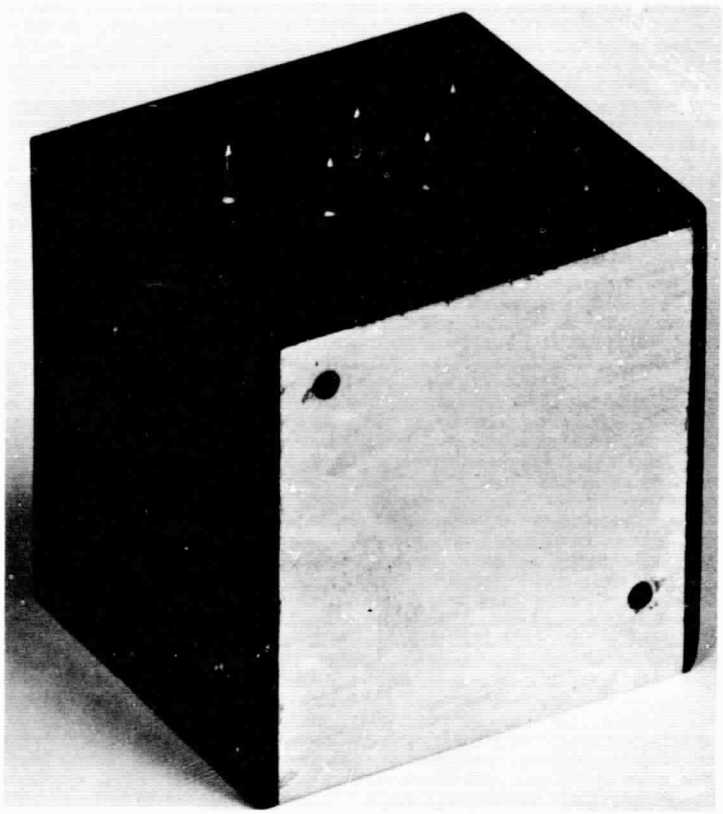


Figure 19. Inverter Module

The power supply contains two thin film substrates with their discrete component cards, five additional discrete component cards, and nine input-output filters. Unlike the other module types, the power supply (Figures 20 and 21) is totally enclosed in aluminum for EMI protection. Three power transistors are mounted on a heat sink bracket in much the same manner as are those in the inverter module.

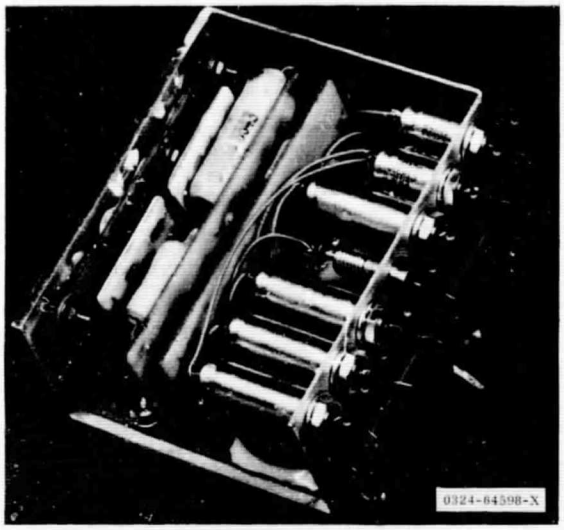


Figure 20. Power Supply Module (Unencapsulated)

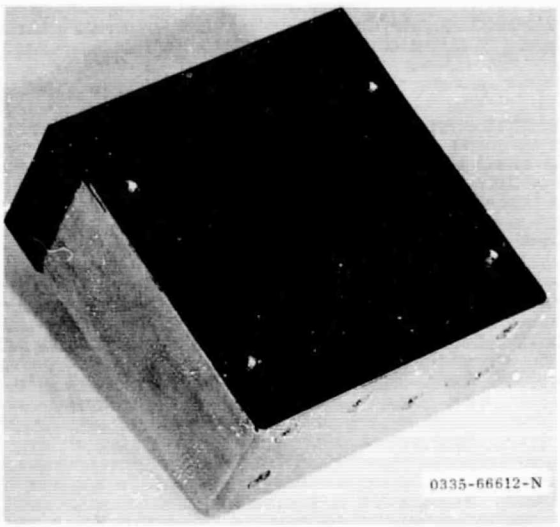


Figure 21. Power Supply Module

All the modules have a common height of 1.4 inches. This allows them to plug into the channel interconnection card and also to be screwed to the machined casting, thereby creating a structural sandwich. In addition, the power supply module (3.0 by 3.2 by 1.4 inches), which occupies approximately 25 percent of the channel interconnection card area, is screwed to the card in four places, thereby contributing substantially to the structural integrity of the channel assembly.

III. MANUFACTURING

A. THIN FILM MICROCIRCUIT FABRICATION

1. Basic Engineering Requirements

a. Substrate Fabrication

Thin film resistors and conductors were deposited on American Lava Corporation Alsimag 614 ceramic substrates with 743 glaze (Part No. CT-60401-M). Substrate size is 1.0 ± 0.010 by 1.0 ± 0.010 by 0.030 ± 0.005 inch.

Thin film resistor values ranged from 5 ohms to 100,000 ohms. Tolerances on resistor values, indicated on the schematic diagrams, ranged from ±1 to ±5 percent. Temperature coefficient of resistance was a maximum of ±50 parts per million per degree centrigrade for all thin film resistors.

Conductors had a maximum resistivity of 0.03 ohms per square over a temperature range of -55°C to +150°C. Conductor pads had a gold surface suitable for thermocompression bonding of gold wire up to 0.003 inch diameter, and a minimum size of 0.030 by 0.030 inch.

Power loading for ±1 percent resistors was restricted to a maximum of 50 watts per square inch. All other resistors were permitted a power loading of no more than 150 watts per square inch.

b. Substrate Acceptance Tests

Substrates were required to meet the following performance requirements both before and after nonoperating storage for 500 hours at +150°C and temperature cycling from -55°C to +150°C for 24 hours.

1. Substrate resistors will have a temperature coefficient of resistance less than ±50 parts per million per degree centrigrade over a temperature range of -55°C to +150°C and resistance values at +25°C within the tolerances specified on the schematic diagrams.

2. Substrate conductors will have a maximum resistivity of 0.03 ohms per square over a temperature range of -55°C to +150°C.

2. Process Development

a. Resistors

Circuits for Phase III were vacuum-deposited in a vacuum system operating in the 10^{-6} Torr region. Chromel C alloy was deposited to a final sheet resistance of 500 ohms per square and over-coated with vacuum deposited pure gold to seal the resistor film during further non-vacuum processing.

b. Conductors

To meet the conductivity requirement of 0.03 ohms per square, a relatively thick deposit of gold was required. This was applied by electrodeposition from a cyanide gold bath (Martin Standard Process P31001F).

The process sequence for the fabrication of thin film circuits for Phase III is shown below.

1 Vacuum Deposition (Thin Film Portion)

a Vacuum deposit chromel C resistor layer over entire substrate to a nominal value of 25 percent below final desired value;

b Vacuum deposit a protective layer of pure gold conductor (approximately 5000Å);

2 Plating - Electrodeposit 40,000Å gold for high conductivity circuits;

3 Etching

a Photoetch the composite circuit (resistors and conductors) all the way down to the substrate to determine conductor geometry and resistor widths;

b Photoetch resistor areas selectively, uncovering resistors and establishing their lengths;

4 Passivation

a Measure resistors and adjust to ±1 percent; passivation occurs to prevent further oxidation;

b Check resistors for TCR and tolerance at 25°C and 150°C;

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b Photoetch resistor areas selectively, uncovering resistors and establishing their lengths;

4 Passivation

a Measure resistors and adjust to ±1 percent; passivation occurs to prevent further oxidation;

b Check resistors for TCR and tolerance at 25°C and 150°C;

5 Sealing

a Vacuum deposit 10,000Å of silicon oxide over resistor areas (six green (Wratten 74) interference color cycles is the method used to monitor thickness);

b Burn-in for 20 hours at 150°C and recheck temperature coefficient of resistance and tolerance;

c Spray coat with Electroscience 44H silicone coating, masking areas where bonds are to be made. Dry at room temperature for 20 minutes, and cure for 2 hours at 150°C.*

3. Protective Coatings

As described in the Phase II Completion Report, the Phase III substrate assemblies were fabricated using an auxiliary PC card spaced 0.010 inch above the thin film. An analysis of those modules which failed at the thin film level revealed that the basic cause was contamination of the film by solder flux and residues, causing electrochemical corrosion. Because of the closely spaced packaging configuration, it became obvious that a conformal coating over the thin film substrate was necessary in order to properly protect the film. A silicone electronic protective coating, Electroscience Laboratories No. 44H, was selected for use in Phase III. It was applied to the properly masked circuit by spray coating then air dried and oven cured as indicated in the process sequence. Since the replacement modules protected by the silicone coating were placed in the system, no further failures due to corrosion have been observed. In addition, thin film test substrates were coated with the silicone and subjected to 20 temperature cycles, -55 to +125°C, under electrical load at rated wattage. No resistor changes in excess of 0.3 percent were observed. Aging of silicone coated test circuits at 150°C with activated flux applied also produced no change in film properties.

B. MODULE FABRICATION AND ASSEMBLY

1. Thin Film Hybrid Assembly

A two-level microcircuit technique, consisting of a 1 by 1 inch PC board and a 1 by 1 inch thin film resistor network, was used in the thin film hybrid assembly. The PC card and thin film substrate details (Figure 22 a-b) were bonded together at several locations in a fixture main-

*This step was developed after Phase III modules were failure analyzed and was used on replacement and spare modules.

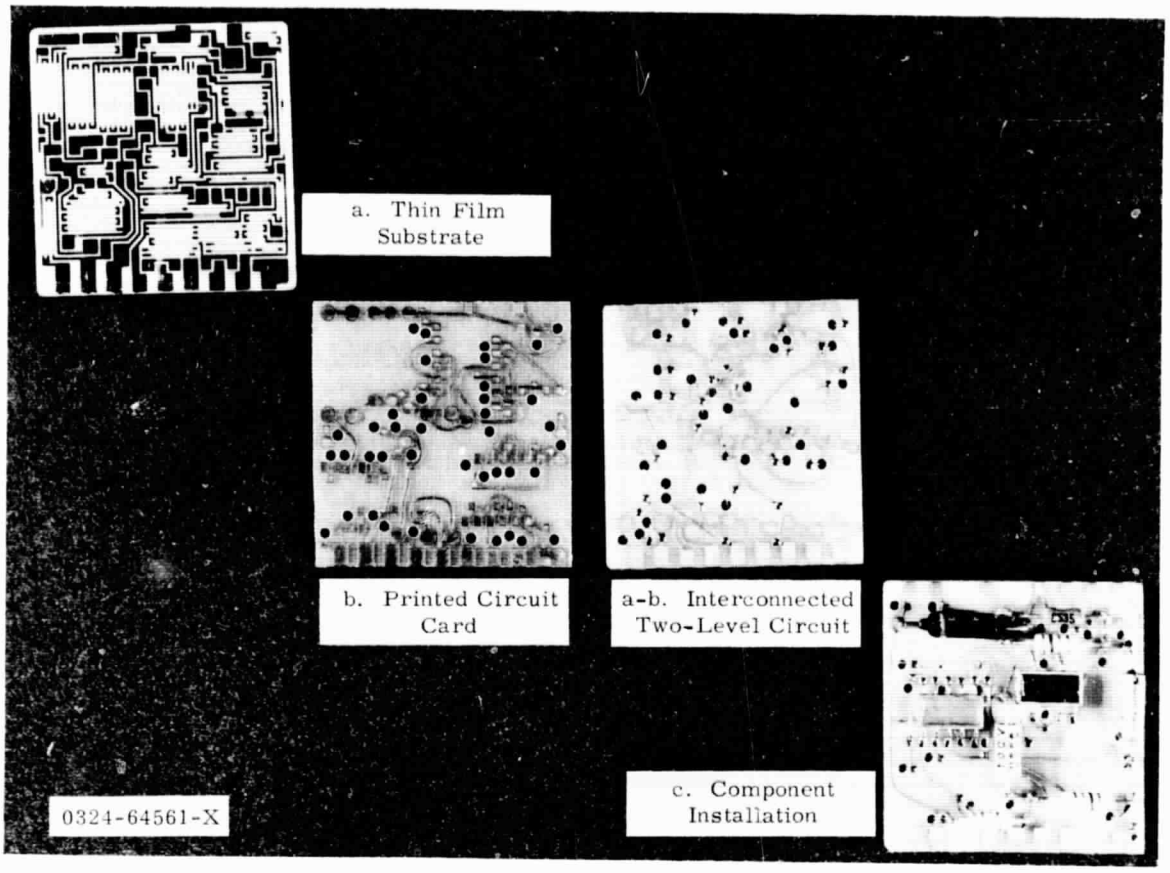


Figure 22. Printed Circuit Card and Thin Film Substrate Details

taining 0.010 inch spacing between. This spacing is necessary to clear any jumpers used to bond in spare resistors on the thin film substrate and to protect the finish of the deposited elements and conductors. Interconnecting wires 0.002 inch in diameter were then bonded to appropriate pad areas on the thin film substrate through a 0.040 inch diameter clearance hole in the PC board. The wire is then formed over to a termination pad on the PC board and bonded to complete the interconnection. At this point, all discrete components are attached to the PC board using conventional microsoldering techniques (Figure 22c and Figure 23). Output pins are soldered in place and the assembly flush-cleaned in alcohol for flux residue removal preliminary to electrical t ts.

a. Joining Techniques

Through experimentation, a 0.002 inch diameter gold plated OFHC annealed copper wire was chosen for its compatibility with the materials and joining techniques involved in the hyb. .d assembly described above.

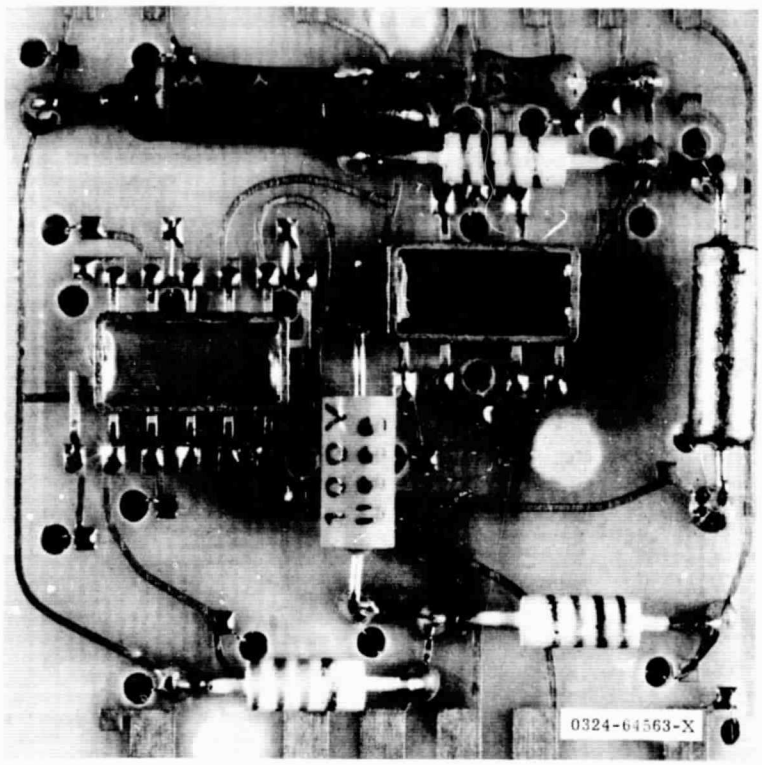


Figure 23. Details of Component Installation

The methods of interconnections selected were thermocompression bonding to thin film and soldering to printed circuit boards. Bonds to the thin film substrate surface were made with a parallel gap microwelder head equipped with moly electrodes and a constant voltage power supply with controlled energy pulse duration.

The components were soldered after the interconnections were made to the thin film circuit. These components are hand formed and butt soldered to the PC pads with solder preforms and heat controlled microsoldering irons. Input-output leads of 0.012 inch diameter gold plated Dunet wire were attached to PC board and then soldered to the PC pads.

b. Joint Strength

1) Wire to Thin Film

Preliminary pull tests of the 0.002 inch gold plated OFHC annealed wire bonded to gold conductors were recorded as follows:

1 Pulls at 0 degree shear broke base material;

2 Pulls at 45 degree peel broke lead in heat-affected zone, leaving bond;

3 Pulls at 90 degree peel broke the bond and left copper in bonded areas.

The tensile strength of the 0.002 inch OFHC annealed copper wire used in these tests was 55 grams which is approximately twice the strength of a 0.002 inch pure gold wire used in conventional thermocompression bonding.

2) Preliminary Temperature Aging

Similar pull-tests were conducted on joints bonded to thin film substrates after subjection to 150°C for 100 hours. No appreciable change in results was noted using the same pulling attitude.

3) Solder Joints

The butt solder joints have proven to be reliable and no problems have been encountered. The spacing during PC board layout controls the soldering of components to avoid remelting the previously soldered interconnections.

c. Protective Coating

The thin film hybrid circuits were tested and conformally coated with Dow Corning RTV 503 silicone rubber component. This coating serves as a protective coat for the small diameter wire and components and allows further encapsulating without damage to components.

2. Component PC Boards

Some small component boards necessary for assembly of discrete components, transformers, and power transistors, were used in the modules. Conventional soldering techniques were used and no problems were encountered.

3. Micromodule Assembly

The thin film hybrid circuits and discrete component boards were assembled into a module. The number of thin film circuits varied from two to eight per module. Interconnections were made by a PC board located at the base of the module and by cross wire welding at the top. In the cross wire welding, the 0.012 inch diameter pure nickel cross wires were welded to the 0.012 inch diameter Dunet risers.

The module outputs were mounted on the base header board and then soldered. The assembled module was then tested over the temperature range of -55 to +125°C. After testing, the module was encapsulated with Minnesota Mining & Manufacturing CRP-241, a semiflexible, filled epoxy compound. After encapsulation the module was again tested.

4. Rework

If a failure occurred during test, the module was taken apart and the individual thin film hybrid circuits and component boards placed on a test fixture for evaluation. This was possible because of the use of RTV 503 and the encapsulation material. All failures that occurred during this phase were evaluated, resulting in solutions to some of the basic problems.

IV. ENVIRONMENTAL TEST RESULTS

A. TEMPERATURE TESTS

The objective of the thermal tests of the ACSP was to verify the operation of the unit at heat sink temperatures of -55 to +105°C. The +105°C temperature was determined by the module operating temperature (+125°C) minus the calculated temperature rise from the heat sink to the hottest module. Actual measurements have since indicated a thermal rise of 12°C in the prototype. The prototype heat sink was maintained, as closely as possible, at the oven ambient temperature by welding eight radiating vanes to the heat sink mounting plate. Measurements indicated a thermal rise of less than 5°C above the oven ambient. The ACSP was allowed to stabilize at 105°C for 5 hours and at -55°C for 2 hours.

Functional data were recorded with the results shown in Tables I through VI. Tables I through III are the high temperature results and Tables IV through VI are the low temperature results. The tests for low and high temperatures were not conducted at the same time because of the scheduling of other environmental tests. This is the reason for two sets of +25°C readings. The unit operated within specifications over the temperature range with the exception of two comparators and one rate switch. In each case, the failure mode was determined and is shown by the notes at the bottom of the table. These failures include one jumper connection and two poorly sealed substrate resistors.

Modifications have been made to prevent a recurrence of these types of failures in future modules. The modifications include a new type of substrate sealing material and changes in the manner of connecting the PC cards to the substrate.

B. EMI TESTS

During the design phase of the ACSP, the problems revealed by EMI tests made on the CSP system were carefully considered. Consequently, such design practices as single point grounding, line filters, shielded modules, shield cables, and by-pass networks were utilized in the design of the ACSP and provided favorable EMI results. The EMI tests performed on the ACSP were in accordance with MIL-I-6181D. The results of each type of test are listed as follows.

TABLE I

Channel 1 High Temperature Results

Demodulator

Temp (°C)	Input (V rms)	Reference TM (Volts) Phase 0°	Reference TM (Volts) Phase 180°	Command TM (Volts) Phase 0°	Command TM (Volts) Phase 180°	Standby (Volts) Phase 0°	Standby (Volts) Phase 180°
+25	2V	0.990	0.990	1.004	1.004	44.900	44.920
	1V	0.498	0.498	0.503	0.503	22.480	22.510
	0	0.000	0.000	0.000	0.000	0.007	0.007
+105	2V	1.002	1.002	0.995	0.993	44.892	44.892
	1V	0.502	0.502	0.498	0.498	22.500	22.500
	0	0.000	0.000	0.000	0.000	0.000	0.000

Comparator*

Temp (°C)	Command Threshold Phase 0° (mV rms)	Command Threshold Phase 180° (mV rms)	Reference Threshold Phase 0° (mV rms)	Reference Threshold Phase 180° (mV rms)
+25	324	333	331	328
+105	274	387	None	None

Wheel Speed

Temp (°C)	Threshold Frequency (Hz) Roll High	Roll Low	Yaw High	Yaw Low	Pitch High	Pitch Low
+25	1656	1555	1658	1554	1658	1554
+105	1661	1556	1665	1553	1663	1555

Rate Switch

Temp (°C)	Input (V rms)	Reference Threshold (V rms) Phase 0°	Reference Threshold (V rms) Phase 180°	Command TM (Volts) Phase 0°	Command TM (Volts) Phase 180°	Command Threshold (V rms) Phase 0°	Command Threshold (V rms) Phase 180°	Standby Threshold (V rms) Phase 0°	Standby Threshold (V rms) Phase 180°
+25	4V	3.994	4.003	4.992	4.977	4.011	4.025	4.009	4.017
	2V	2.00[illegible]	2.015	2.504	2.488	2.008	2.021	2.004	2.014
	0			0.010	0.010				
+105	4V	3.994	3.999	4.974	4.958	4.034	4.049	4.011	4.030
	2V	2.009	2.021	2.500	2.480	2.012	2.027	1.995	2.009
	0			0.012	0.012				

Power Supply

Temp (°C)	+27 Volts	-27 Volts	+18 Volts
+25	26.949	26.9[illegible]0	18.252
+105	26.869	26.806	18.340

Inverter

Temp (°C)	V_{out} rms	Freq (Hz)	Dist %
+25	25.894	401.3	1.45
+105	25.855	401.6	1.12

*Open thin film resistor on comparator substrate.

TABLE II

Channel 2 High Temperature Results

Demodulator								Comparator				
		Reference TM (Volts) Phase		Standby (Volts) Phase		Command TM (Volts) Phase			Reference Threshold Phase		Command Threshold Phase	
Temp (°C)	Input (V rms)	0°	180°	0°	180°	0°	180°	Temp (°C)	0° (mV rms)	180° (mV rms)	0° (mV rms)	180° (mV rms)
	2V	0.989	0.989	44.940	44.900	0.995	0.995	+25	327	324	326	327
+25	1V	0.496	0.496	22.500	22.500	0.498	0.498	+105	327	325	326	326
	0	0.000	0.000	0.004	0.004	0.000	0.000					
	2V	1.003	1.002	44.870	44.840	0.998	0.991					
+105	1V	0.502	0.501	22.500	22.460	0.500	0.496					
	0	0.000	0.000	0.020	0.020	0.000	0.000					

Wheel Speed						
	Threshold Frequency (Hz)					
	Roll		Yaw		Pitch	
Temp (°C)	High	Low	High	Low	High	Low
+25	1651	1547	1650	1546	1647	1548
+105	1664	1552	1661	1555	1660	1555

Rate Switch										Power Supply			
		Reference				Standby		Command		Temp (°C)	+27 Volts	-27 Volts	+18 Volts
		TM (Volts) Phase		Threshold (V rms) Phase		Threshold (V rms) Phase		Threshold (V rms) Phase		+25	26.982	26.887	18.269
Temp (°C)	Input (V rms)	0°	180°	0°	180°	0°	180°	0°	180°	+105	26.834	26.758	18.386
	4V	4.984	4.970	4.006	4.015	4.023	4.031	4.018	4.020				
+25	2V	2.500	2.487	1.996	2.006	2.010	2.019	2.003	2.004				
	0	0.010	0.010										
	4V	4.990	4.975	3.997	4.006	4.015	4.029	4.032	4.049				
-105	2V	2.503	2.486	2.005	2.021	2.000	2.014	2.011	2.027				
	0	0.020	0.020										

Inverter			
Temp (°C)	V_{out} rms	Freq (Hz)	Dist %
+25	25.975	399.9	1.25
+105	25.864	401.3	1.20

TABLE III

Channel 3 High Temperature Results

Demodulator

Temp (°C)	Input (V rms)	Command TM (Volts) Phase 0°	Command TM (Volts) Phase 180°	Reference TM (Volts) Phase 0°	Reference TM (Volts) Phase 180°	Standby (Volts) Phase 0°	Standby (Volts) Phase 180°
+25	2V	1.000	1.000	0.998	0.998	44.910	44.930
	1V	0.500	0.501	0.499	0.499	22.500	22.500
	0	0.000	0.000	0.000	0.000	0.006	0.006
+105	2V	0.997	0.997	0.996	0.998	44.840	44.890
	1V	0.499	0.499	0.497	0.498	22.440	22.470
	0	0.000	0.000	0.000	0.000	0.018	0.018

Comparator

Temp (°C)	Command Threshold Phase 0° (mV rms)	Command Threshold Phase 180° (mV rms)	Reference Threshold Phase 0° (mV rms)	Reference Threshold Phase 180° (mV rms)
+25	329	328	328	327
+105	327	331	297*	303*

Wheel Speed

Temp (°C)	Threshold Frequency (Hz) Roll High	Roll Low	Yaw High	Yaw Low	Pitch High	Pitch Low
+25	1654	1549	1654	1549	1654	1549
+105	1656	1551	1656	1551	1657	1551

Rate Switch

Temp (°C)	Input (V rms)	Command Threshold (V rms) Phase 0°	Command Threshold (V rms) Phase 180°	Reference Threshold (V rms) Phase 0°	Reference Threshold (V rms) Phase 180°	Standby TM (Volts) Phase 0°	Standby TM (Volts) Phase 180°	Standby Threshold (V rms) Phase 0°	Standby Threshold (V rms) Phase 180°
+25	4V	4.022	4.036	3.999	4.016	4.982	4.970	4.010	4.023
	2V	2.001	2.018	1.997	2.014	2.498	2.483	2.011	2.023
	0					0.012	0.012		
+105	4V	4.047	4.055	4.027	4.050	4.975	4.966	4.022	4.031
	2V	1.999	2.028	1.997	2.019	2.494	2.485	2.008	2.016
	0					0.009	0.009		

Power Supply

Temp (°C)	+27 Volts	-27 Volts	+18 Volts
+25	26.918	26.887	18.043
+105	26.789	26.752	18.158

Inverter

Temp (°C)	V_{out} rms	Freq (Hz)	Dist %
+25	26.143	399.4	1.30
+105	26.117	400.1	0.90

*Drift caused by change in resistor value on comparator substrate due to improper sealing.

TABLE IV

Channel 1 Low Temperature Results

Demodulator								Comparator				
		Reference TM (Volts) Phase		Command TM (Volts) Phase		Standby (Volts) Phase			Command Threshold Phase		Reference Threshold Phase	
Temp (°C)	Input (V rms)	0°	180°	0°	180°	0°	180°	Temp (°C)	0° (mV rms)	180° (mV rms)	0° (mV rms)	180° (mV rms)
+25	2V	0.997	0.998	0.998	0.998	44.857	44.875	+25	327.5	328.7	326.2	326.1
	1V	0.499	0.499	0.500	0.500	22.480	22.496	-55	328.4	328.4	327.0	326.3
	0	0.000	0.000	0.000	0.000	0.008	0.008					
-55	2V	0.994	0.995	0.995	0.996	44.750	44.780					
	1V	0.498	0.498	0.499	0.499	22.410	22.410					
	0	0.000	0.000	0.000	0.000	0.016	0.016					

Wheel Speed						
	Threshold Frequency (Hz)					
	Roll		Yaw		Pitch	
Temp (°C)	High	Low	High	Low	High	Low
+25	1649	1550	1651	1549	1655	1547
-55	1540	1547	1641	1546	1646	1540

Rate Switch									
		Reference		Command				Standby	
		Threshold (V rms) Phase		TM (Volts) Phase		Threshold (V rms) Phase		Threshold (V rms) Phase	
Temp (°C)	Input (V rms)	0°	180°	0°	180°	0°	180°	0°	180°
+25	4V	4.014	4.030	5.003	4.982	3.999	4.015	4.010	4.023
	2V	1.998	2.019	2.509	2.489	2.000	2.014	2.012	2.026
	0			0.013	0.013				
-55	4V	4.035	4.052	4.970	4.951	4.021	4.036	4.012	4.056
	2V	2.008	2.023	2.492	2.476	2.022	2.034	2.003	2.048
	0			0.009	0.009				

Power Supply			
Temp (°C)	+27 Volts	-27 Volts	+18 Volts
+25	26.942	26.908	18.008
-55	27.103	27.074	17.921

Inverter			
Temp (°C)	V_{out} rms	Freq (Hz)	Dist %
+25	26.036	400.0	2.00
-55	26.132	400.3	2.90

TABLE V

Channel 2 Low Temperature Results

Demodulator								Comparator				
Temp (°C)	Input (V rms)	Reference TM (Volts) Phase 0°	Reference TM (Volts) Phase 180°	Standby (Volts) Phase 0°	Standby (Volts) Phase 180°	Command TM (Volts) Phase 0°	Command TM (Volts) Phase 180°	Temp (°C)	Reference Threshold Phase 0° (mV rms)	Reference Threshold Phase 180° (mV rms)	Command Threshold Phase 0° (mV rms)	Command Threshold Phase 180° (mV rms)
+25	2V	0.989	0.989	44.940	44.920	0.997	0.998	+25	327.6	327.1	326.1	325.3
	1V	0.495	0.495	22.527	22.473	0.499	0.499	-55	327.5	327.8	327.1	325.4
	0	0.000	0.000	0.010	0.010	0.000	0.000					
-55	2V	0.989	0.989	44.870	44.840	0.997	0.997					
	1V	0.495	0.495	22.495	22.490	0.499	0.500					
	0	0.000	0.000	0.007	0.007	0.000	0.000					

Wheel Speed						
	Threshold Frequency (Hz)					
Temp (°C)	Roll High	Roll Low	Yaw High	Yaw Low	Pitch High	Pitch Low
+25	1656	1550	1657	1549	1655	1550
-55	1647	1542	1647	1543	1645	1545

Rate Switch									
		Reference				Standby		Command	
Temp (°C)	Input (V rms)	TM (Volts) Phase 0°	TM (Volts) Phase 180°	Threshold (V rms) Phase 0°	Threshold (V rms) Phase 180°	Threshold (V rms) Phase 0°	Threshold (V rms) Phase 180°	Threshold (V rms) Phase 0°	Threshold (V rms) Phase 180°
+25	4V	4.968	4.945	5.171*	5.175*	4.012	4.022	4.022	4.029
	2V	2.490	2.470	1.997	2.015	2.002	2.016	2.010	2.016
	0	0.012	0.012						
-55	4V	4.996	4.992	3.305*	3.309*	4.039	4.048	4.018	4.029
	2V	2.499	2.499	1.993	1.993	2.022	2.032	2.006	2.015
	0	0.001	0.001						

Power Supply			
Temp (°C)	+27 Volts	-27 Volts	+18 Volts
+25	26.937	27.134	18.787
-55	27.086	27.246	18.710

Inverter			
Temp (°C)	V_{out} rms	Freq (Hz)	Dist %
+25	25.890	400.5	2.18
-55	25.957	400.1	2.50

*Broken jumper to rate switch threshold pot.

TABLE VI

Channel 3 Low Temperature Results

Demodulator								Comparator				
		Command TM (Volts) Phase		Reference TM (Volts) Phase		Standby (Volts) Phase			Command Threshold Phase		Reference Threshold Phase	
Temp (°C)	Input (V rms)	0°	180°	0°	180°	0°	180°	Temp (°C)	0° (mV rms)	180° (mV rms)	0° (mV rms)	180° (mV rms)
25	2V	1.001	1.002	1.000	1.001	45.070	45.070	+25	327.7	327.1	327.3	327.6
	1V	0.501	0.502	0.501	0.502	22.590	22.590	-55	328.9	326.8	327.0	328.7
	0	0.000	0.000	0.000	0.000	0.010	0.010					
-55	2V	1.000	1.001	1.000	1.000	45.000	45.010					
	1V	0.501	0.501	0.501	0.502	22.600	22.610					
	0	0.000	0.000	0.000	0.000	0.007	0.007					

Wheel Speed						
	Threshold Frequency (Hz)					
	Roll		Yaw		Pitch	
Temp (°C)	High	Low	High	Low	High	Low
+25	1656	1545	1656	1545	1653	1548
-55	1644	1542	1646	1540	1642	1544

Rate Switch									
		Command		Reference		Standby			
		Threshold (V rms) Phase		Threshold (V rms) Phase		TM (Volts) Phase		Threshold (V rms) Phase	
Temp (°C)	Input (V rms)	0°	180°	0°	180°	0°	180°	0°	180°
+25	4V	3.996	4.006	4.006	4.019	4.994	4.979	4.022	4.033
	2V	2.006	2.014	1.997	2.009	2.506	2.490	2.008	2.020
	0					0.010	0.010		
-55	4V	4.035	4.042	4.064	4.069	4.993	4.986	4.013	4.017
	2V	2.015	2.023	2.050	2.055	2.502	2.493	2.013	2.021
	0					0.007	0.007		

Power Supply			
Temp (°C)	+27 Volts	-27 Volts	+18 Volts
+25	26.848	26.815	18.677
-55	26.982	26.967	18.570

Inverter			
Temp (°C)	V_{out} rms	Freq (Hz)	Dist %
+25	26.070	400.9	1.40
-55	26.068	400.5	2.10

1. Radiated Interference

Radiation from the ACSP (all channels operating) cable and interconnecting wires from 0.15 to 1000 MHz was measured as specified by MIL-I-6181D. A plot of the measurements are shown in Figure 24. The levels are well within the acceptance limits with the exception of a small portion of the band from 0.15 to 0.5 MHz.

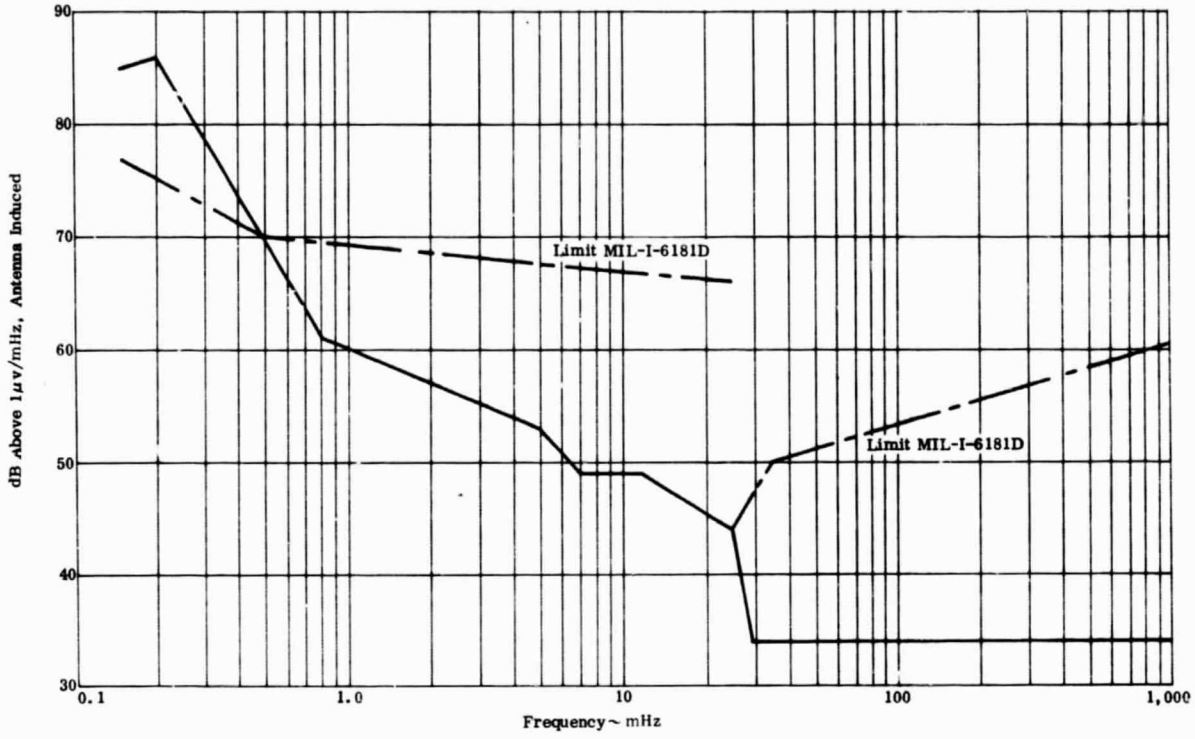


Figure 24. Broadband Radiated Interference Measurements

2. Radio Frequency Radiated Susceptibility

In this test the ACSP was subjected to a radio frequency field from 0.15 to 1000 MHz. This field was established with a 50 ohm signal generator driving an appropriate antenna and matching network at a 0.1 volt open circuit level. No change in indications, malfunction, or degrac on of performance was observed on the ACSP system.

3. Audio Susceptibility

A 3 volt rms signal from 50 tc 15,000 Hz was applied to the ACSP 28 volt input power leads (Reference Figure 19 of MIL-I-6181D). No change in indication, malfunction, or degradation of performance was observed on the ACSP system.

4. Conducted Interference on Power Leads

In this test, radio frequency voltages generated by the ACSP from 0.15 to 25 MHz were measured using a line stabilization network in each power line (Reference Figure 11 of MIL-I-6181D). The test was performed on each channel of the ACSP and the ACSP system. Test results for each channel are shown by the curves of Figure 25, which are well within the acceptance limits. Test results for the ACSP system are shown in Figure 26 and indicate some peaks above the acceptable limits for a small portion of the band.

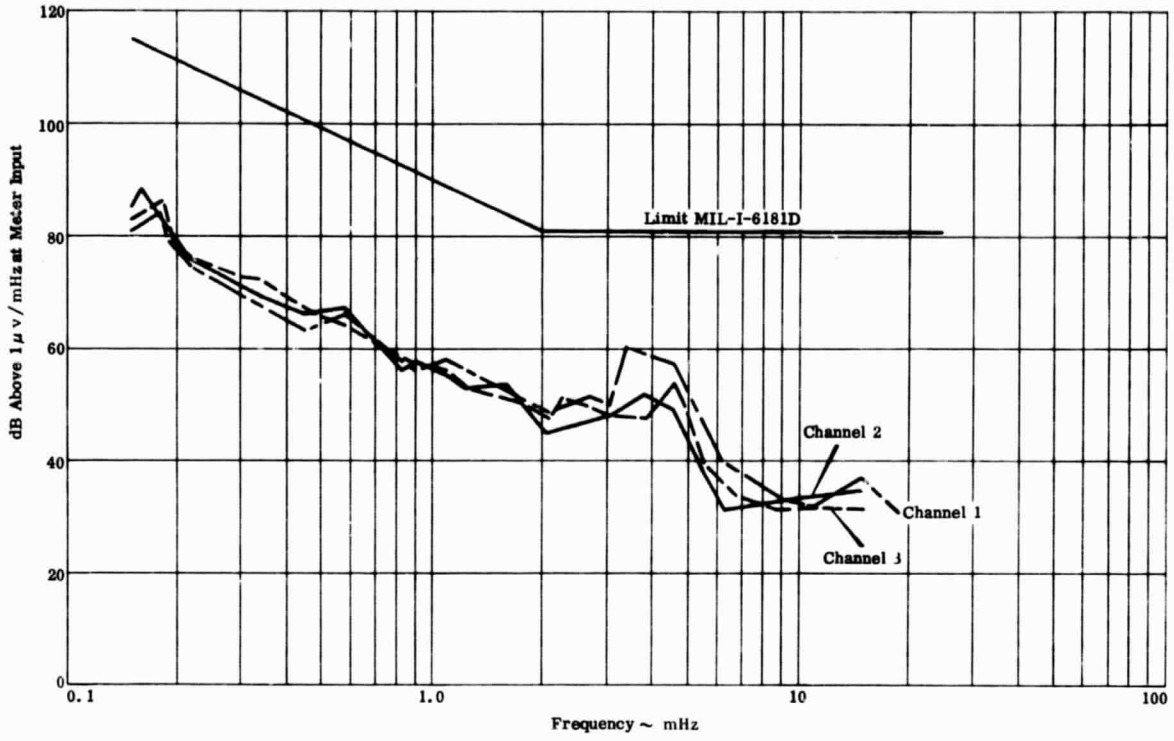


Figure 25. Broadband Conducted Interference Measurements on Power Line of Each Channel

5. Conducted Interference on Output Cable

The conducted interference on the output cable is tested in the same setup as the conducted interference on power leads except that a current probe is placed around the output cable. Figure 27 shows the test results for each channel. Channel 1 displayed a 4 dB peak above the acceptable level at 2.2 MHz. Figure 28 shows the results of the ACSP output cable. A large portion of the band is approximately 20 dB above the acceptable level, apparently indicating that the conductive interference of each channel

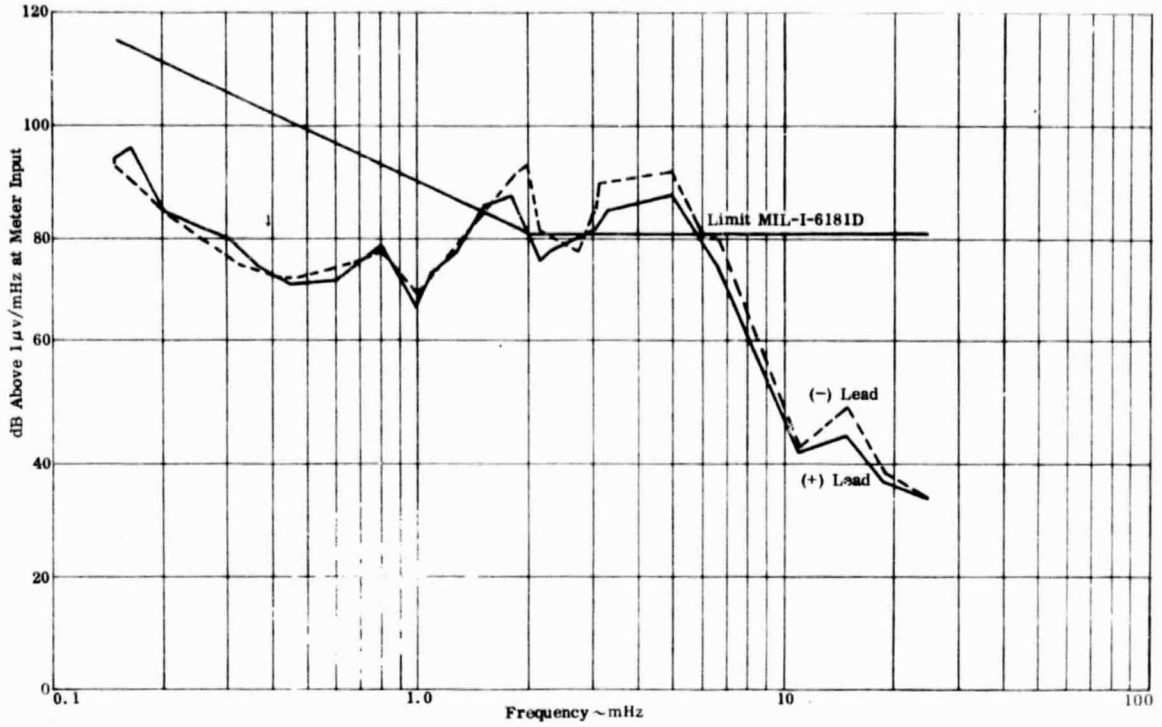


Figure 26. Broadband Conducted Interference Measurements on Power Line Leads of ACSP System

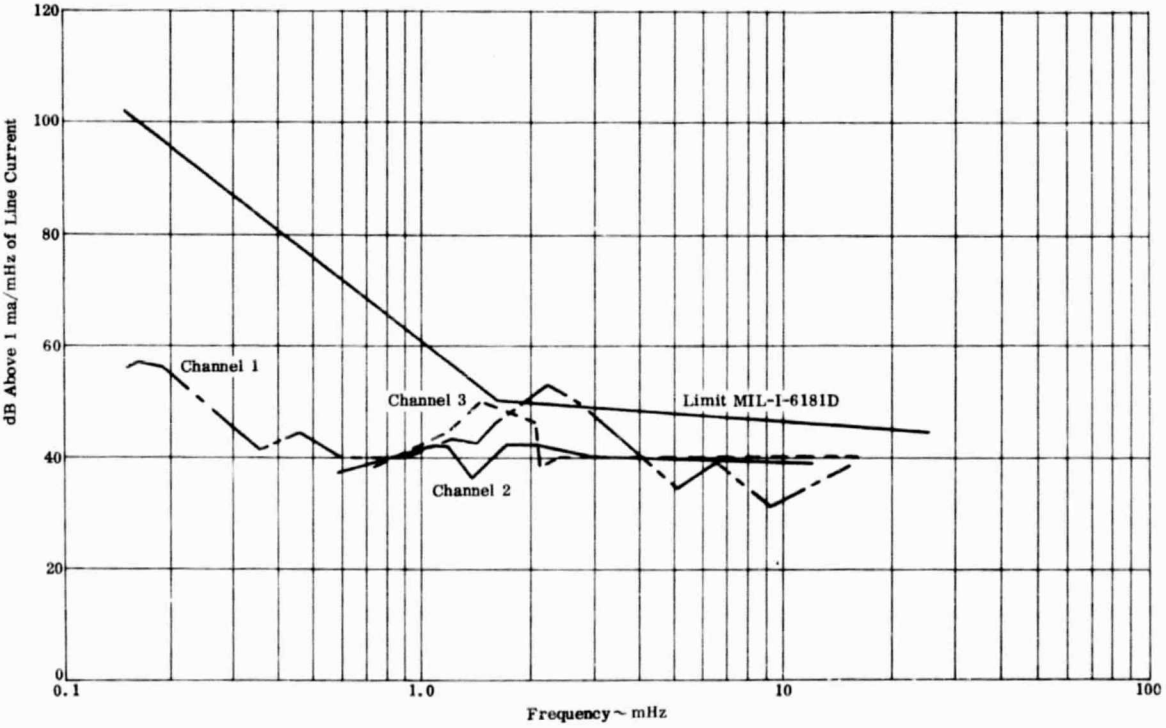


Figure 27. Broadband Conducted Interference Measurements with Current Probe of Each Channel

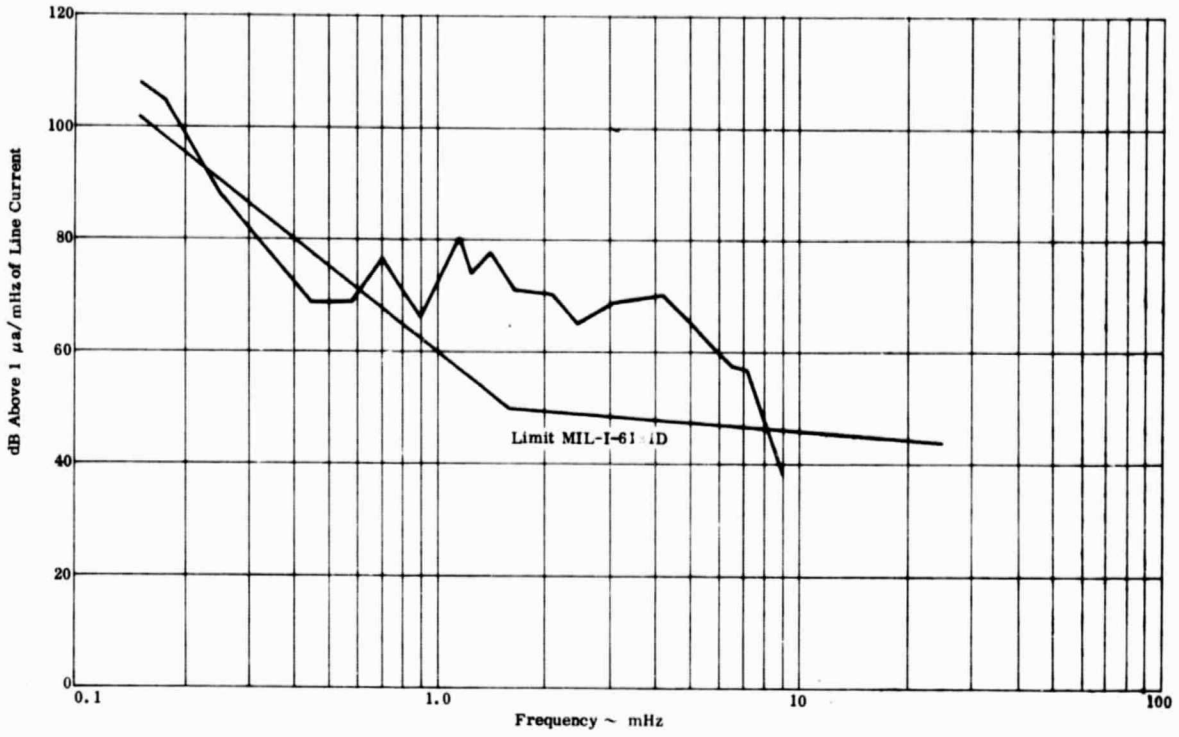


Figure 28. Broadband Conducted Interference Measurements with Current Probe of ACSP System

is summed in the cable. It appears therefore, that a different cable arrangement should be used for future ACSP design. Separate cables for power leads, instrumentation, and output leads should be used to help reduce the conducted interference to acceptable levels. In future designs, such cable separation will be given greater consideration with respect to the conducted interference problems.

C. LEAKAGE TESTS

The contractual requirement is that final pressure in the ACSP enclosure must not decrease to less than 14.7 psi from an initial pressure of 20 psi over a 2 year period with the box in a vacuum.

1. Leakage Rate Calculations

$$P_t = P_0 \exp(-kt)$$

$$14.7 = 20 \exp(-2k)$$

$$\ln 14.7 = \ln 20 - 2k$$

$k = 1/2 (\ln 20 - \ln 14.7) = 0.154$

Volume of gas in ACSP enclosure = 2450 cc

$$P_t = P_0 \exp(-kt)$$

$$\frac{dP_t}{dt} = -k P_0 \exp(-kt)$$

At t = 0:

$$\frac{dP}{dt} = -k P_0 = -0.154 P_0 \text{ psi per year (initial rate of pressure loss)}$$

$$\therefore \left.\frac{dV}{dt}\right|_{\substack{t=0 \\ P=20 \text{ psi}}} = 0.154 V_0 \text{ (initial equivalent volume change)}$$

$$P_1 V_1 = K$$

$$20 \times 2450 = 49{,}000 = K$$

$$V_2\Big|_{P=14.7 \text{ psi}} = \frac{49{,}000}{14.7} = 3333 \text{ cc (equivalent volume at 14.7 psi)}$$

$$\frac{dV}{dt} = 0.154 \times 3333 = 511 \text{ cc/year (at P = 14.7 psi initially)}$$

$$= \frac{511}{3600 \times 24 \times 365} = 1.62 \times 10^{-5} \text{ standard cc/s for nitrogen}$$

$$\frac{1.62 \times 10^{-5}}{0.55} = 2.95 \times 10^{-5} \text{ standard cc/s for helium.}$$

2. Measured Leakage Rates

Conditions	Leakage Rate (Std cc/s)
All seals cleaned thoroughly with alcohol	6.4×10^{-8}
All seals dry after two temperature cycles from -55°C to +125°C (measurement made at +125°C)	2.6×10^{-6}
Same as above except measurement made at +25°C	8×10^{-8}

All seals lubricated with high vacuum grease (same seals removed from box, lubricated, and returned to box)	3×10^{-8}
New seals lubricated with high vacuum grease	1×10^{-8}

It is clear from these measurements that the elastomeric seals used in the ACSP provide leakage rates well below the specification level.

D. VIBRATION, SHOCK, AND ACCELERATION TESTS

1. Dynamic Environments

Contractual requirements for design and development of the ACSP are stated in Table VII. Modifications and additions to the requirements, made at NASA direction, are indicated in Table VIII.

TABLE VII

Contractual Requirements

Vibration:	Sinusoidal, 24g (each axis)
Shock:	Each direction of three major axes 35g; 10 ms (triangular), or 35g, 8 ms (1/2 sine), or 35g; 6 ms (square)
Acceleration:	10g each direction of each axis (5 minutes per run)

2. Design and Development Effort

Primary efforts were applied to vibration analyses since the response acceleration levels for that environment were much higher than those anticipated for shock and acceleration. Figure 29 shows the predicted maximum accelerations that would result from the shock and steady accelerations.

Before the availability of hardware, the design concept was reviewed. Items receiving consideration as potential vibration problems were:

1. Babcock relays
2. Mounting bolts and flanges
3. Module connector pins
4. Enclosure/lid interface flange.

TABLE VIII

Modified Requirements

Vibration: Sinusoidal (1 octave/m, 5 to 2000 to 5 Hz, each axis)

0.188 inch DA;	5 to 43 Hz
±18g;	43 to 165 Hz
±24g;	165 to 700 Hz
±13.5g;	700 to 2000 Hz

Random (3 minutes each axis)

0.12 g^2/Hz;	20 to 64 Hz
+9 dB/oct;	64 to 126 Hz
0.88 g^2/Hz;	126 to 700 Hz
-18 dB/oct;	700 to 916 Hz
0.18 g^2/Hz;	916 to 2000 Hz
	(30g rms)

Shock: Two shocks in each direction of three major axes
35g; 8 ms (i/2 sine)

Acceleration: 10g, each direction of each axis (5 minutes per run)

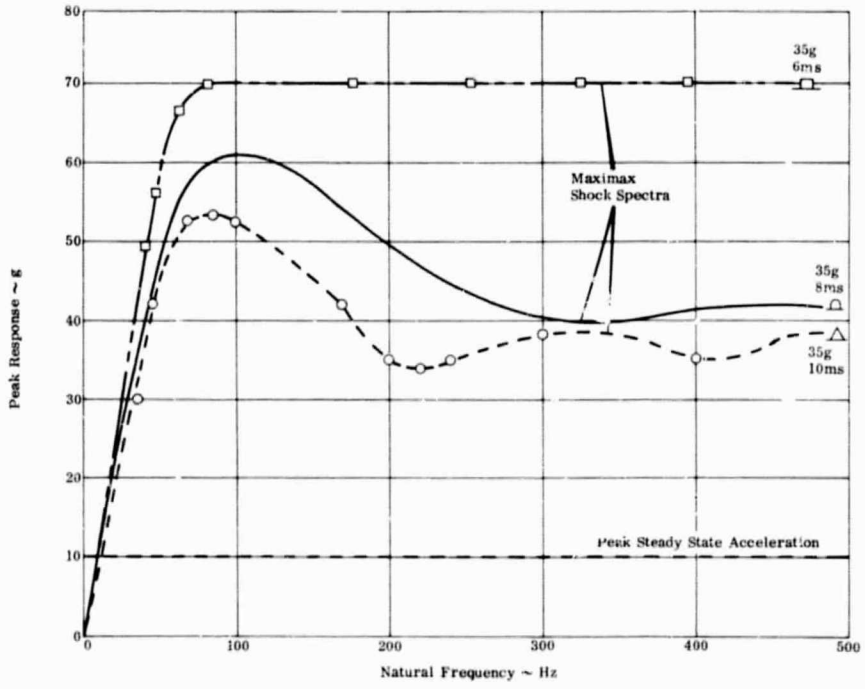


Figure 29. ACSP Environmental Requirements

Fragility levels of all component parts were reviewed. Of these, the Babcock relays were considered most critical. The manufacturer's stated levels for the relays were 0.4 g^2/Hz for 0 to 2000 Hz (28.3g rms) random vibration and 0.4 inch DA for 10 to 40 Hz and ±30g for 40 to 3000 Hz sinusoidal vibration. Since the input requirements for the ACSP were: 1) higher in random vibration (30g rms and 2) 80 percent of the maximum sine level capability of the relay, control and/or attenuation of the response of the box structure would be difficult. Past Martin Company experience with parts of this nature has indicated spectral capabilities much greater than those stated by the manufacturers. To define those capabilities, sinusoidal fragility tests were run on six relays. The results are summarized in Figure 30. Estimated structural responses of the enclosure, frames, and relay connector mounting bar were in the range of 250 to 1000 Hz. Based on these results, the relay environment was not considered critical.

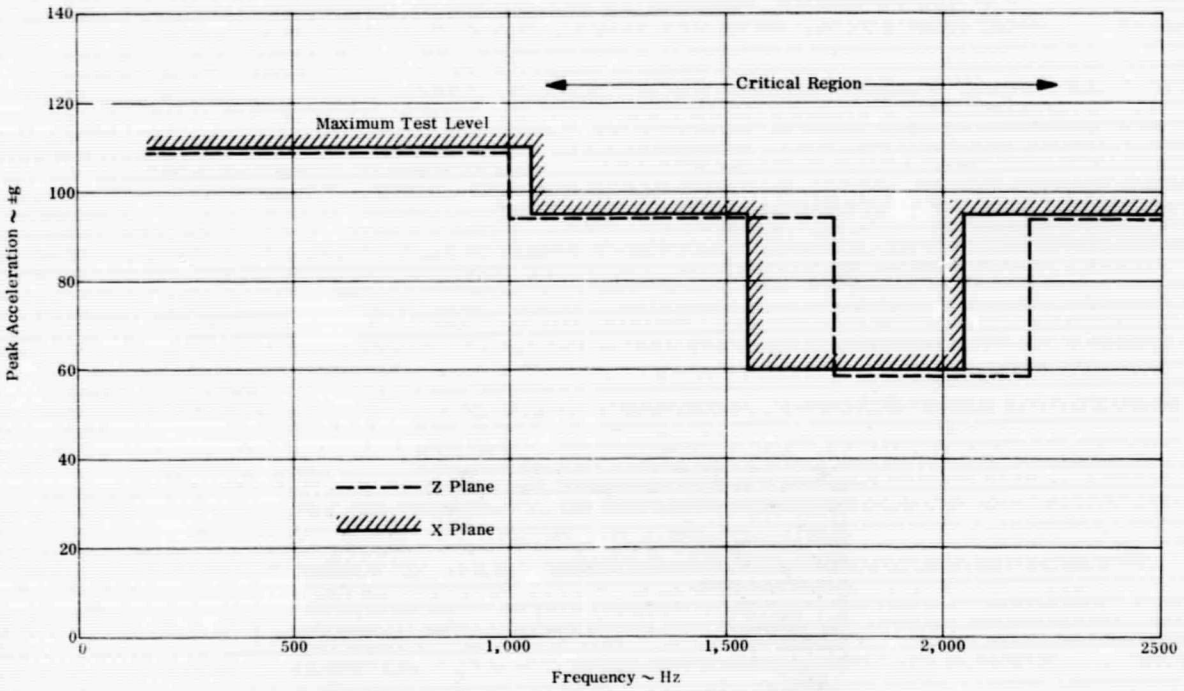


Figure 30. Babcock Relay Fragility Envelope

Analysis of the enclosure mounting flanges resulted in a fundamental bending frequency in the range of 250 to 700 Hz. Using a structural damping characteristic of 0.05, the transmissibility across the flange was estimated as 10/1. At the lower frequencies, this situation was undesirable. Since the flange was difficult to model and the frequency might easily have occurred at the high end of the range, the design was considered marginally acceptable. The significance of the above resonance depended on whether the mounting bolt preload would be exceeded. Analysis indicated that this was possible. Any possibility of a rapid fix to ensure that the preload

would not be overcome was prevented because of direction to use a standard piece of hardware (1/4 inch steel bolt), already stressed to its limit by torqueing.

Analysis of the relative motion across the module connector pins indicated a negligible bending stress in the pin due to an oscillating load created by the printed circuit board. All pins were assumed to share the induced load equally.

To determine possible enclosure-to-lid interface leakage during vibration, a deflection analysis of the span between two of the interface bolts was performed. The span resonant frequency was determined to be much higher than the test range. The preload of the flange surface on the elastomeric seal was great enough to prevent a deflection necessary to allow leakage. This analysis was done to confirm that a reduction in the enclosure flange thickness would not result in leakage during periods of vibration.

3. Developmental Vibration Testing

Initial developmental testing of the ACSP was accomplished using various intensities of both random and sinusoidal excitation. Responses measured during developmental testing were obtained using four subminiature crystal accelerometers located on the ACSP internal structure and two or more standard crystal accelerometers on the outside of the enclosure. The first series of runs were in the Z axis (Figure 31). Vibration responses within the assembly were obtained and are shown in Figures 32 and 33.

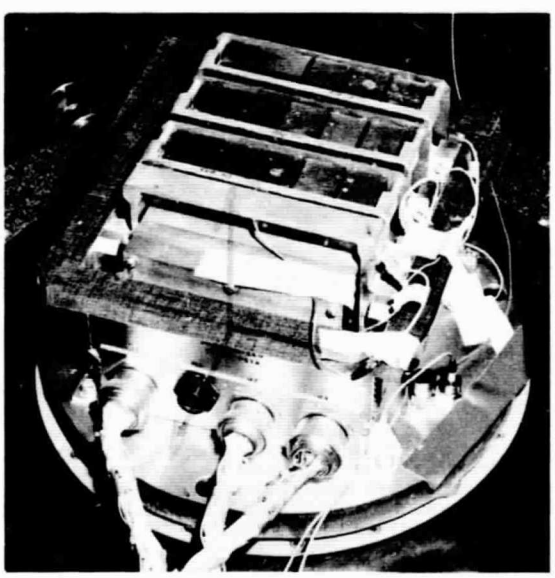


Figure 31. ACSP Reference Axes

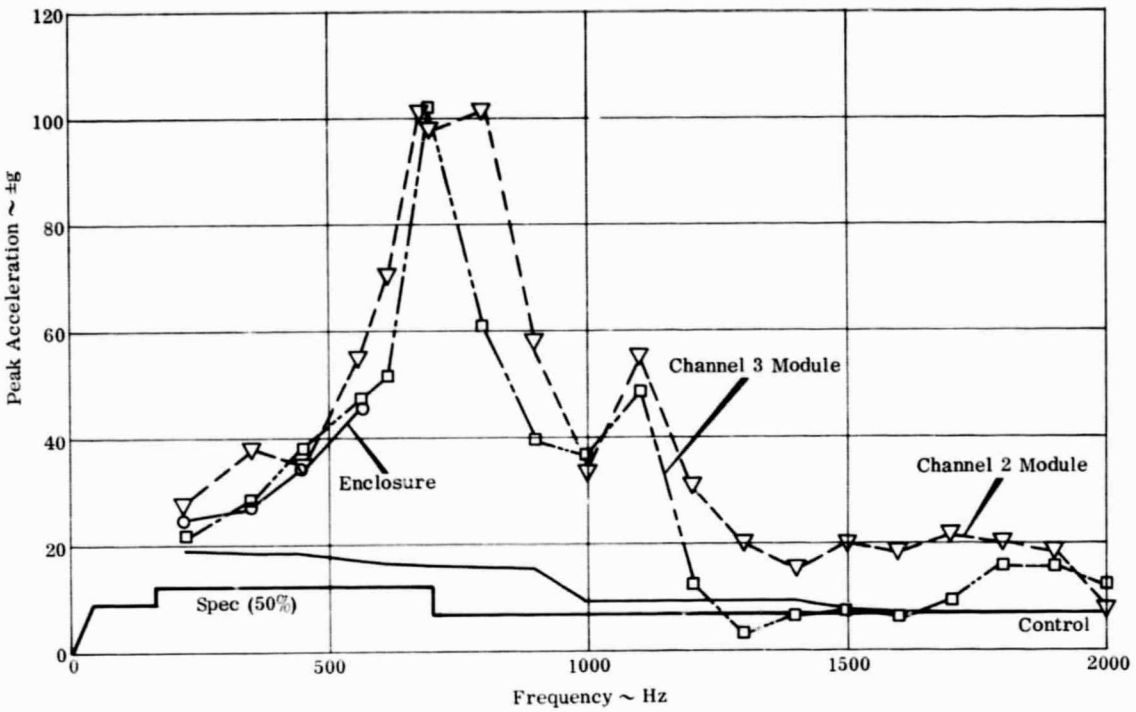


Figure 32. ACSP 50 Percent Sine Test (Upsweep), Z Axis

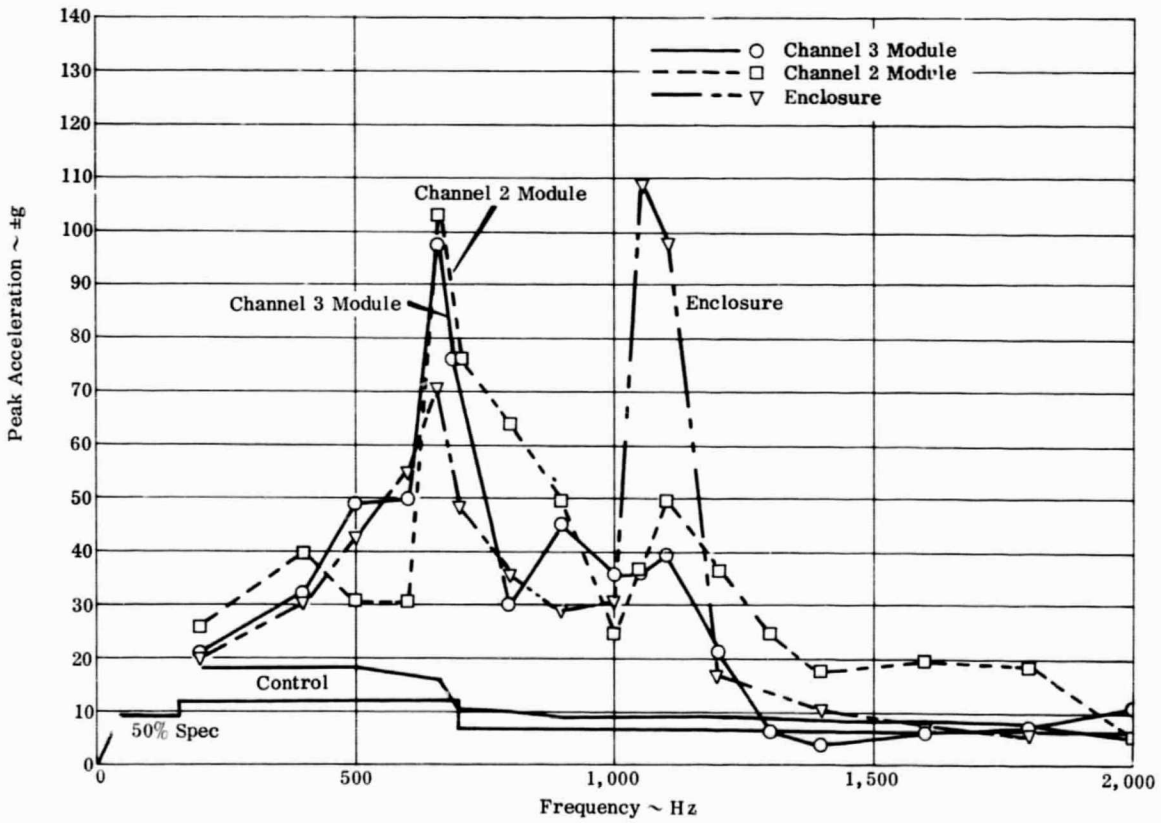


Figure 33. ACSP 50 Percent Sine Test (Downsweep), Z Axis

Nonlinearity of responses within the assembly was not critical enough to warrant further recording of the responses on the downsweep of the excitation. This run confirmed the analysis of the detuning aspects of the relays and the box structure. The high responses on the enclosure and modules directed attention to the amplification across the enclosure mounting flanges. Further runs were made in this axis to better define and confirm the source of this response. Study of the step transmissibilities (i.e., input to enclosure, enclosure to frame, and frame to module obtained and shown in Table IX) confirmed the conclusion. Corrective action recommended involved increasing the mounting pad thickness and adding another gusset to the existing mounting flanges. During these runs malfunctions occurred due to module connector pin breakage, substrate to printed board jumper wire fracture, module component part failures, and edge loaded printed circuit female connectors. At this time, reduction of the high transmissibility across the mounting flange was felt to be sufficient to alleviate most of these problems. Post-test investigation revealed that the printed circuit connector failure occurred because of a combination of excessive preloading and the high response levels. Additional dimensional controls to eliminate any possibility of preload on the connector were imposed to further alleviate the problem.

TABLE IX

Preliminary Z-Axis Step Transmissibilities

Test	Across Mtg Flange	Flange to Enclosure	Input to Enclosure	Enclosure to Frame	Enclosure to Module
5g run (nonpressurized)					
~700 Hz	7/1	0.8/1	5/1	0.9/1	
~1,100 Hz	8/1	0.1/1	0.8/1	1.5/1	
50 percent level sine (pressurized)					
~700 Hz			4/1		1.4/1
~1,100 Hz			11/1*		0.5/1
Full spec level sine					
~700 Hz			4/1	0.5/1	1.5/1
~1,100 Hz			1.5/1	0.8/1	2.8/1

*Location change, attributed to local area enclosure response.

Random vibration excitation of the ACSP showed a more pronounced effect of the failure modes observed in the sinusoidal runs. This was anticipated since in the random phenomenon all resonances are excited concurrently. Curves showing the random input and the responses within the enclosure are shown in Figures 34 through 37.

Sinusoidal vibrations of the unmodified ACSP in the X and Y axes were also performed. The resulting responses are shown in Figures 38 and 39. A summary of this pertinent information retrieved is presented in Table X. A consolidation of the predominant response frequencies, the axis they occurred in, and the probable cause are shown in Table XI.

The ACSP with corrective actions taken to reduce the internal vibration levels was sinusoidally vibrated in the Z axis to evaluate the effect of a rubber pad inserted between the pin end of the modules and the printed circuit boards. Results of these runs indicated that the rubber aggravated the pin breakage problem rather than alleviating it. Significant results of this evaluation are shown in Figure 40.

The results of the modified ACSP structure vibration tests indicated that problems in module pin breakage and module component failures had not been resolved. A decision was made to concentrate further efforts on elimination of the pin breakage problem and reduction of response levels in the ACSP. Failure analysis of the modules at this point showed questionable quality of certain parts and the assembly techniques used in their construction. Both of these situations were being screened by pretest inspection on all modules to be used to reduce problems in further evaluations.

Random vibration tests were conducted on all of the modules to screen out defective ones and to attach a confidence level to the remaining modules for use in subsequent tests. The input vibration levels and spectrum shapes used are presented in Figure 41. These spectrums incorporated dynamic response amplifications encountered within the ACSP enclosure. Previous tests had shown that the random vibration was more severe on the module functional performance than sinusoidal vibration. For this reason, the random screening technique was used.

Analysis of data collected revealed excessive relative deflections of the modules and the PC boards which resulted in loading the structurally weak connector pins. A proposal was accepted to reduce this deflection by increasing the degree of end fixity of the printed board and increasing its moment of inertia and damping characteristic. These objectives were accomplished by removing the six column-type standoffs previously used to support the board and replacing them with welded-in-place continuous standoffs. In addition, a laminated printed board assembly was used in lieu of the former single board.

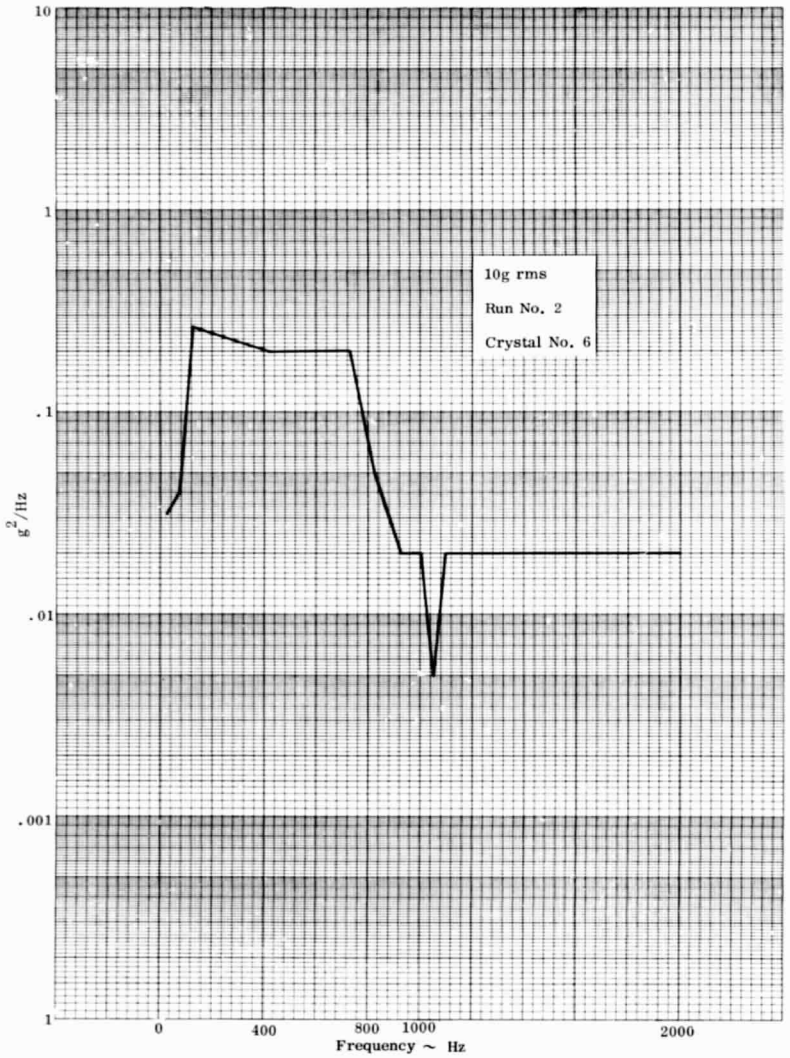


Figure 34. Initial Development, Random Vibration Tests, Controlled Input

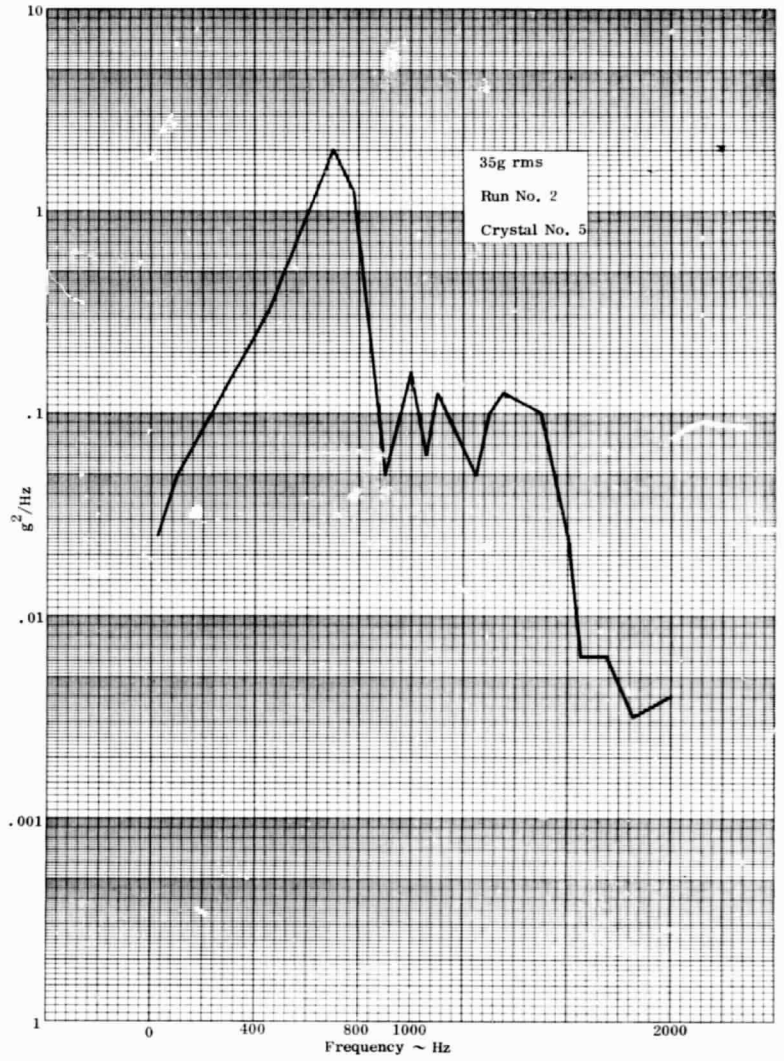


Figure 35. Initial Development, Random Vibration Tests, Enclosure

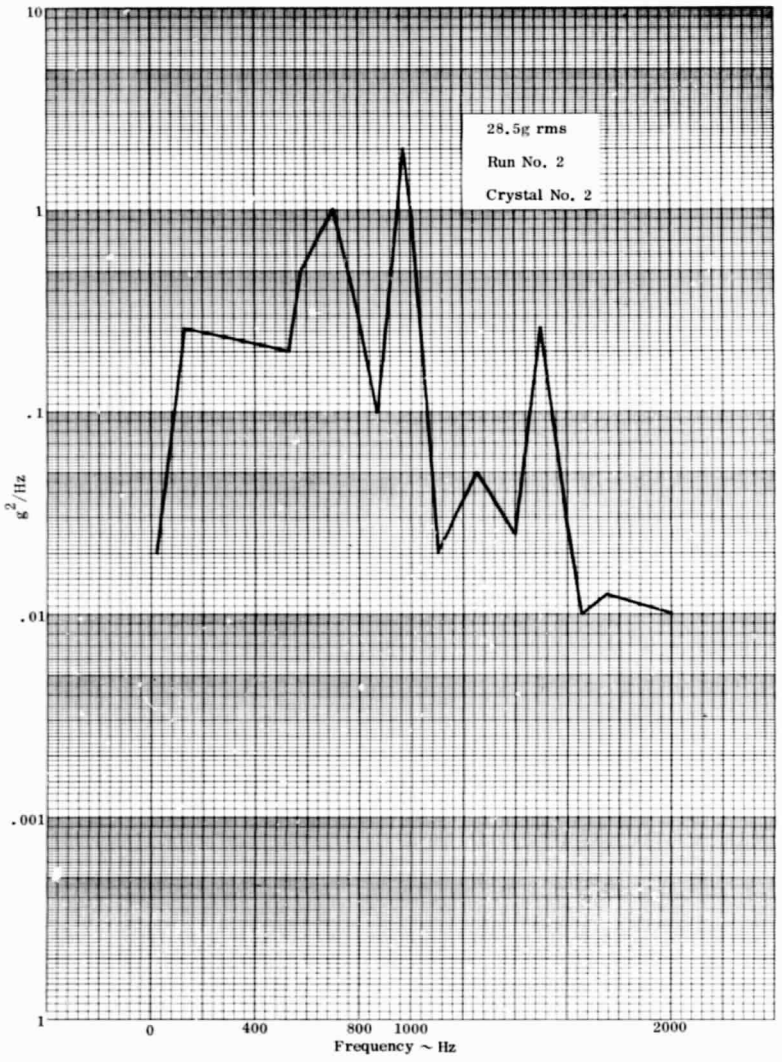


Figure 36. Initial Development, Random Vibration Tests, Channel 2 Module

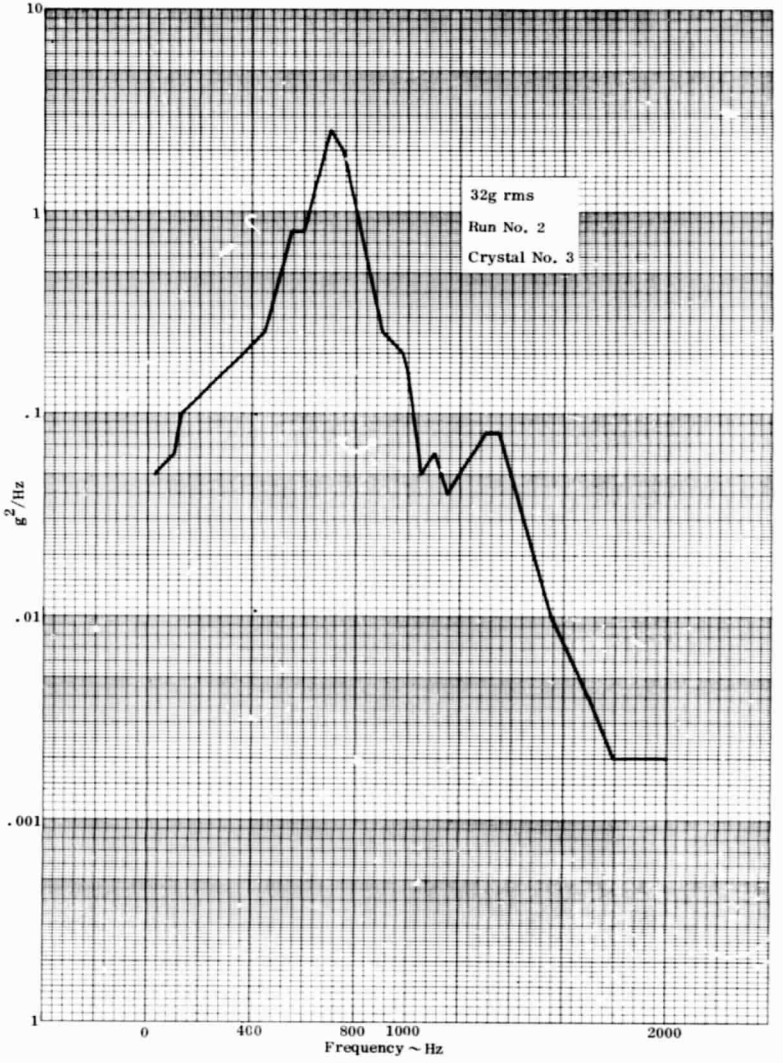


Figure 37. Initial Development, Random Vibration Tests, Channel 3 Module

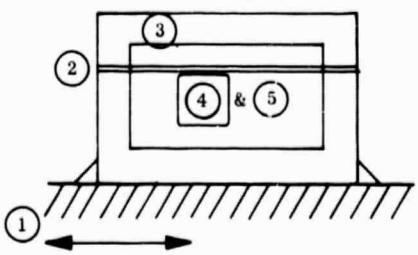
TABLE X

ACSP Step Transmissibilities

Y-Axis (±10g sine sweep run)

	1-2 Input to Enclosure	2-3 Enclosure to Frame	3-4 No. 2 Frame to Demodulator	2-5 Enclosure to Relay Demodulator
(470-500 Hz)	8.2/1	3.2/1	0.4/1	1.7/1

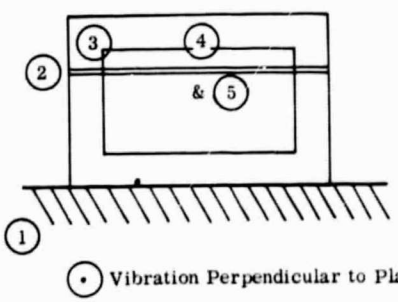
1.3/1



X-Axis (±10g sine sweep run)

	1-2 Input to Enclosure	2-3 Enclosure to No. 2 Frame Side	3-4 Frame Side to No. 2 Frame Midpoint	2-5 Enclosure to Relay Fragmentation Midpoint
400 Hz	8/1	0.5/1	2.5/1	1.3/1
720 Hz	1.4/1	0.3/1	8.5/1	6.5/1*
1,000 Hz	1.7/1	0.2/1	14/1	3.5/1*
1,400 Hz	15/1	0.04/1	3/1	0.01/1

Does not effect interior of ACSP



*Relay frame exhibits similar response 26/1 at 720 Hz, 14/1 at 1000 Hz when using 2-3 transmissibility as typical for all frames.

TABLE XI

ACSP Composite Transmissibilities

Frequency (Hz)	Probable Source
400	Mounting bolts or enclosure (X)
470 to 500	Mounting bolts or enclosure (Y)
700 to 720	Mounting flange (Z) Frame assembly (X)
1,000	Frame assembly (X)
1,050	Mounting flange (Z)
1,400	Enclosure structure (X), not critical

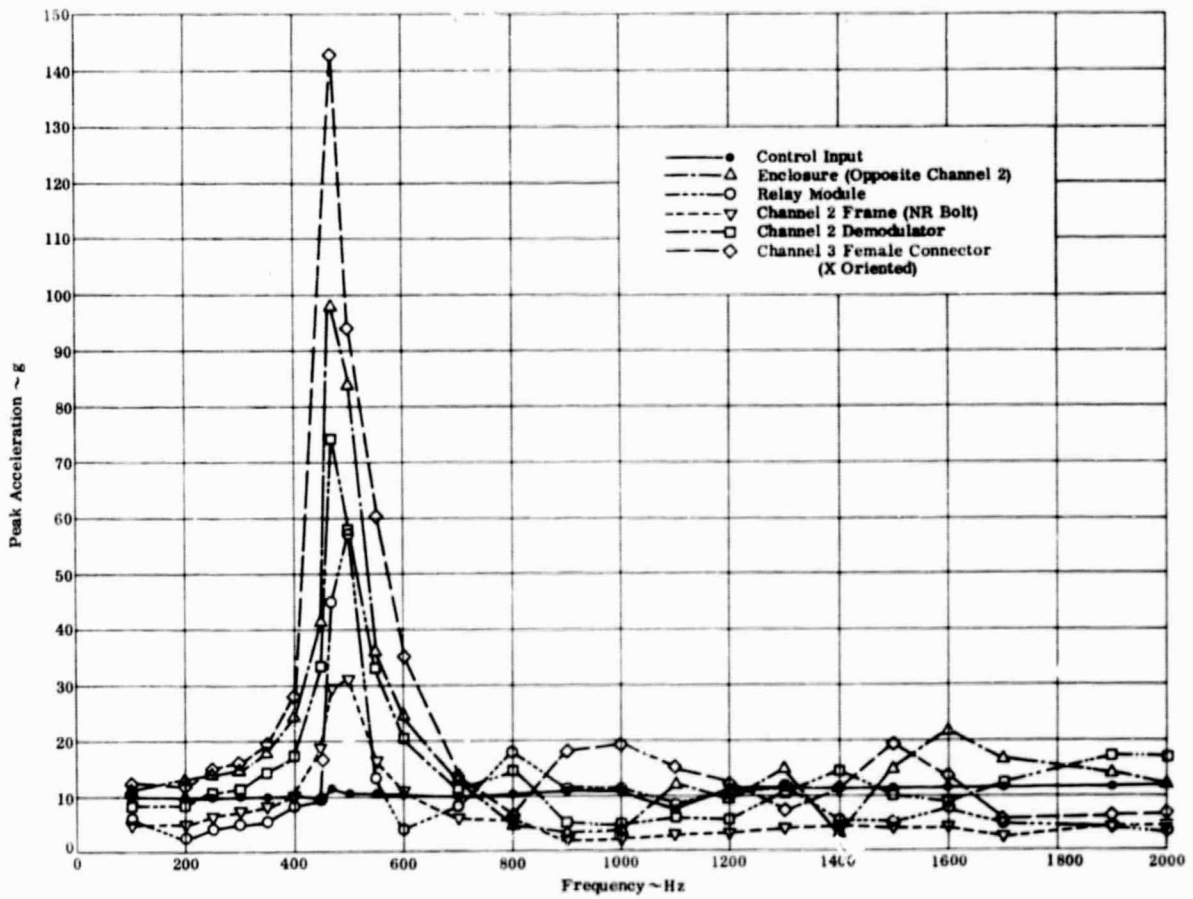


Figure 38. ACSP Sinusoidal Vibrations in Y Axis

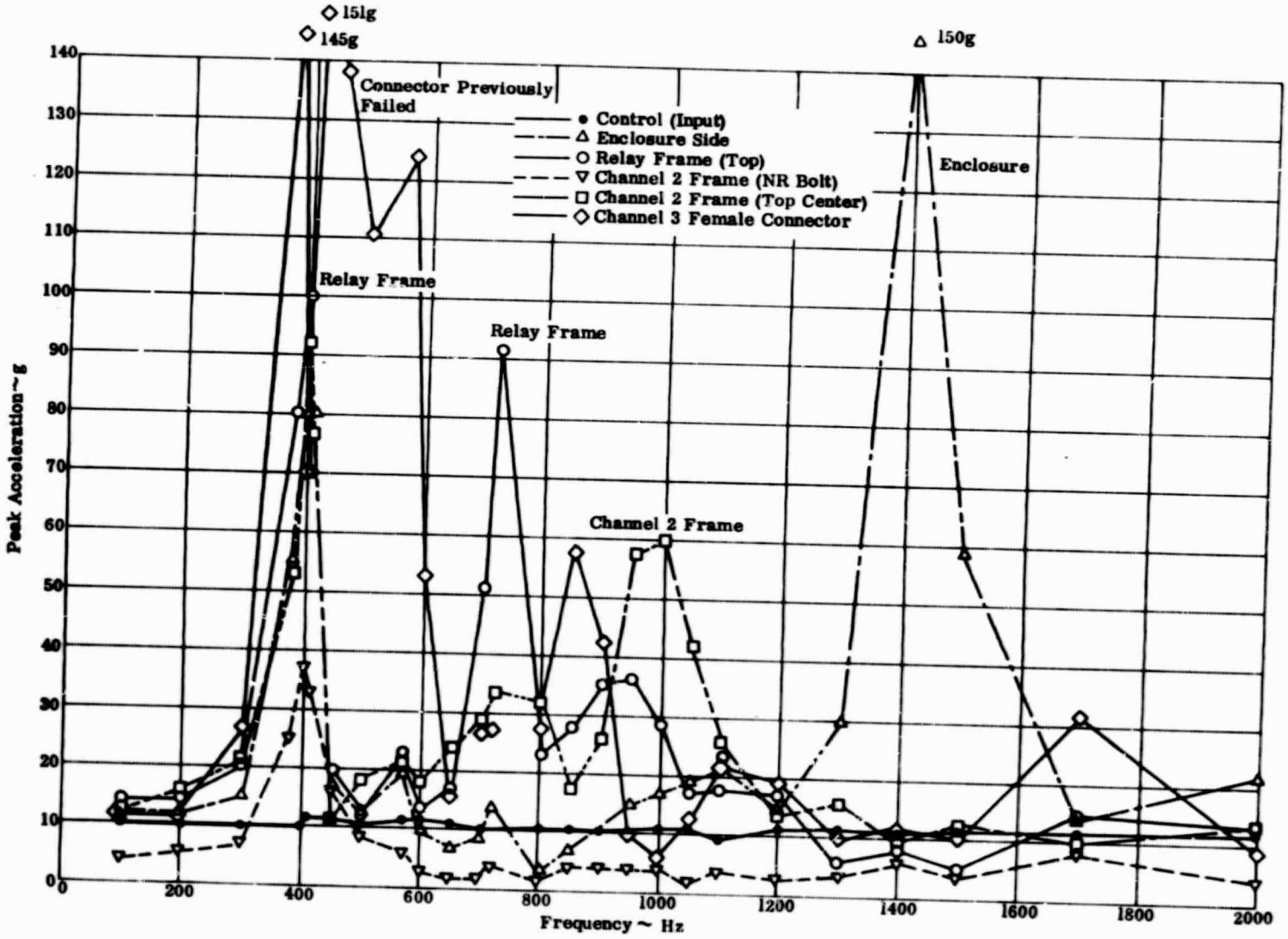


Figure 39. ACSP Sinusoidal Vibrations in X Axis

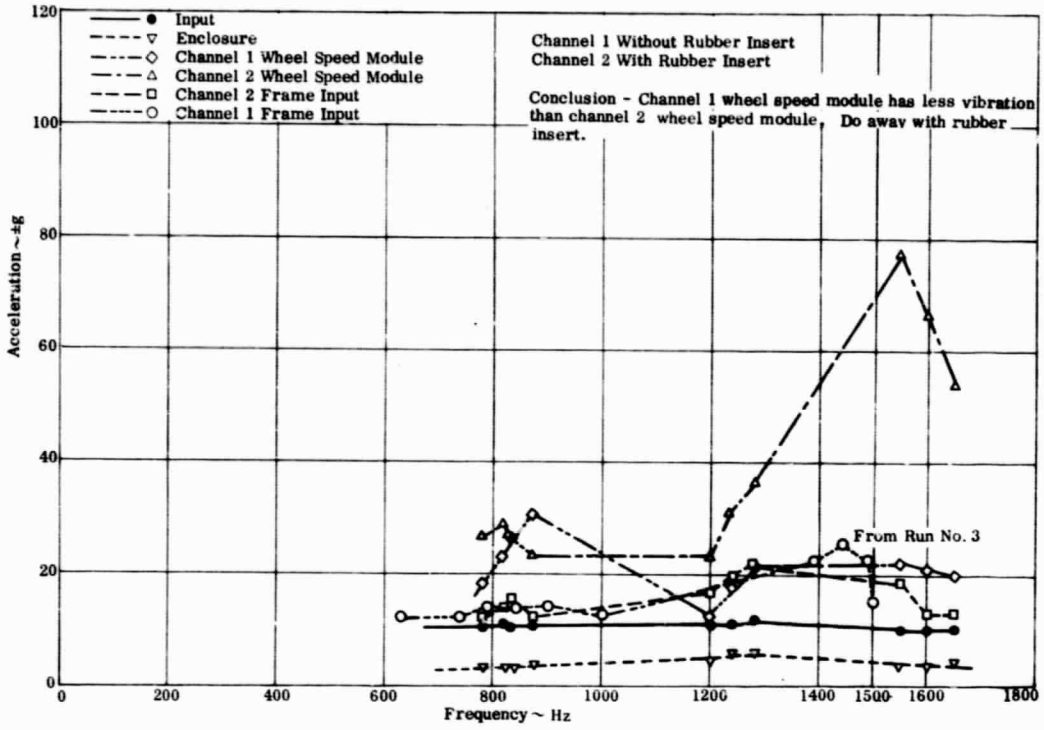


Figure 40. ACSP Rubber Insert Evaluation

Two types of binder material were used between the G-10 and melamine boards, (epoxy and RTU). The dynamic response of the channel assembly to vibration excitation in the X and Z axes, as measured on the assembly frame, PC board, and modules, is presented in Figures 42 through 46. The input vibration was sinusoidal and at the levels prescribed in Table VIII. Not all measurements were recorded in each axis. The effect of the modification on the relative displacement of the pins is presented in Table XII. On the base of these data and successful test results, the epoxy binder was selected as the best. As an additional benefit the epoxy binder assembly showed significant reductions in response in the X axis (perpendicular to the boards) as compared to the RTV assembly and plain board.

The high acceleration levels encountered during developmental testing in the X-axis were attributed to a coupling of the resonant frequencies of the PC board on the channel assembly and of the enclosure. To alleviate this condition, small channels were added along both mounting edges of each PC board. An assembly incorporating this modification was tested to both a sinusoidal and random vibration environment. The dynamic response of the ACSP with the additional channel assembly to the sinusoidal environment is presented in Figures 47 through 49. No appreciable change was noted in the response to X-axis excitation, but the channel assembly resonant frequencies in the Z-axis were raised.

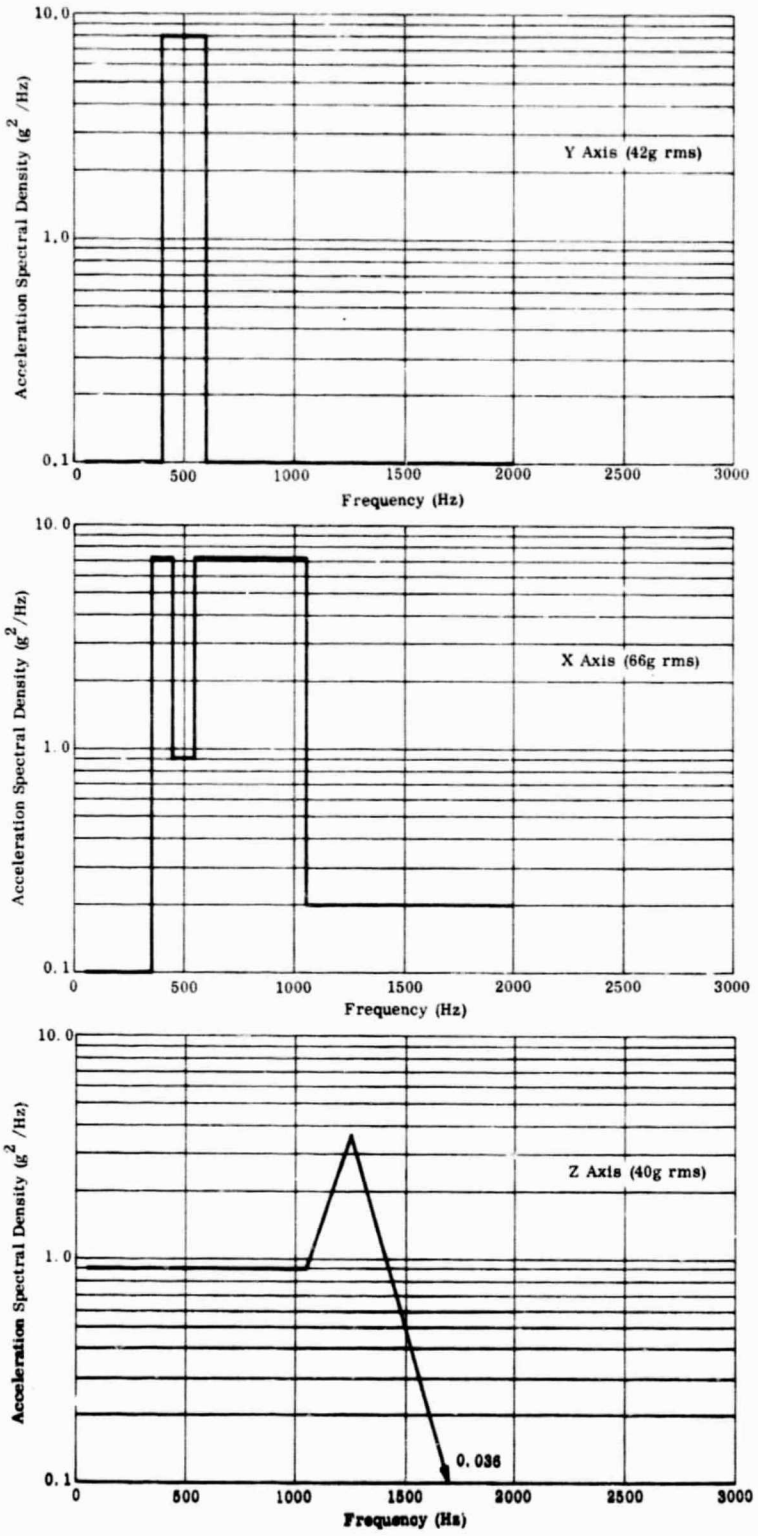


Figure 41. Vibration Spectra for Module Screening

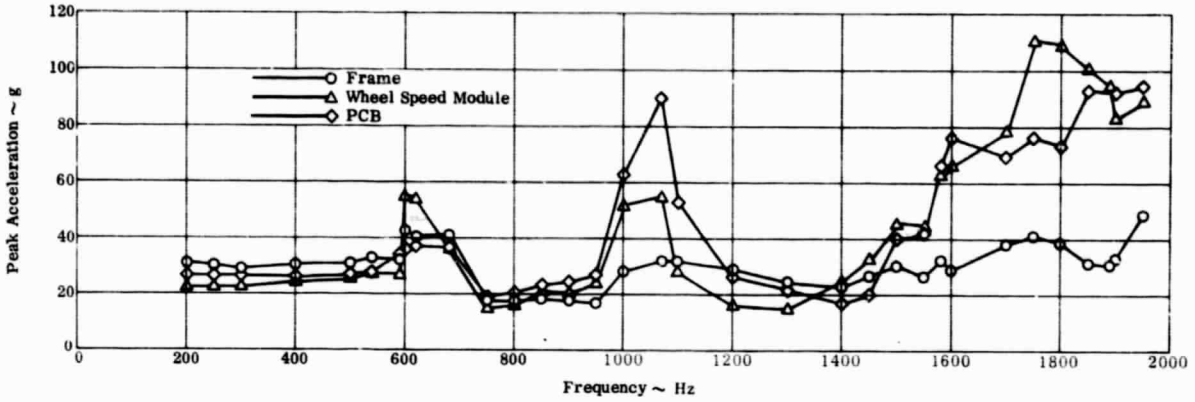


Figure 42. ACSP Z Axis, Plain PCB

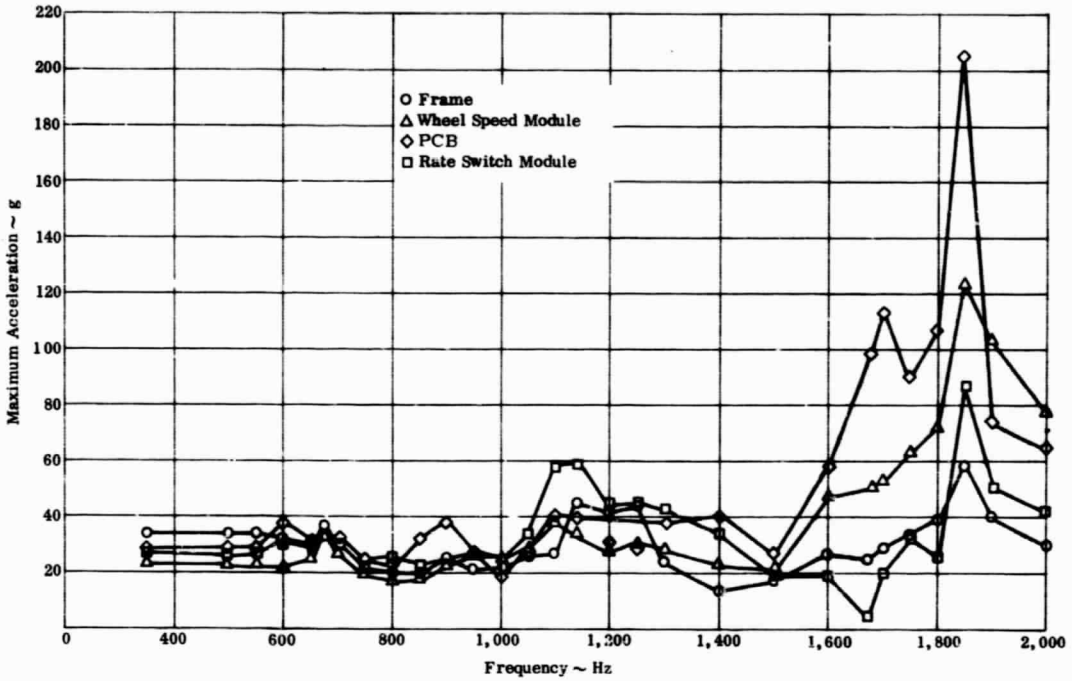


Figure 43. ACSP Z Axis, PCB with RTV

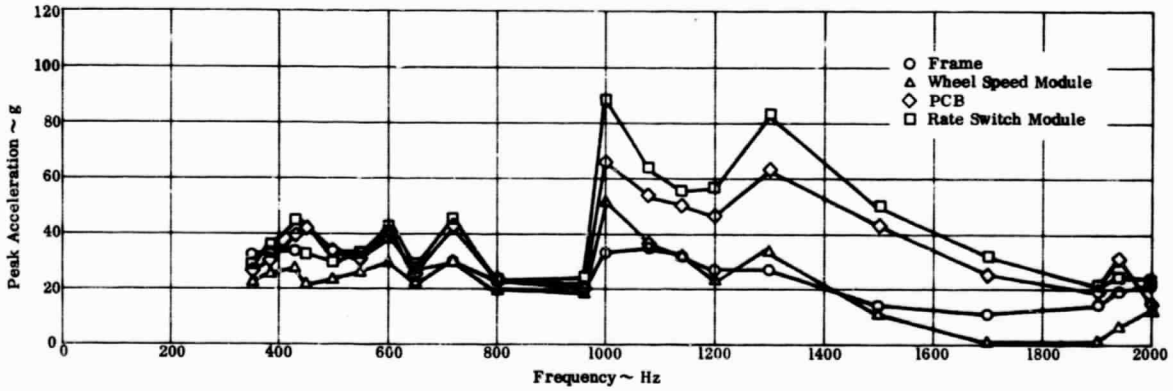


Figure 44. ACSP Z Axis, PCB with Epoxy

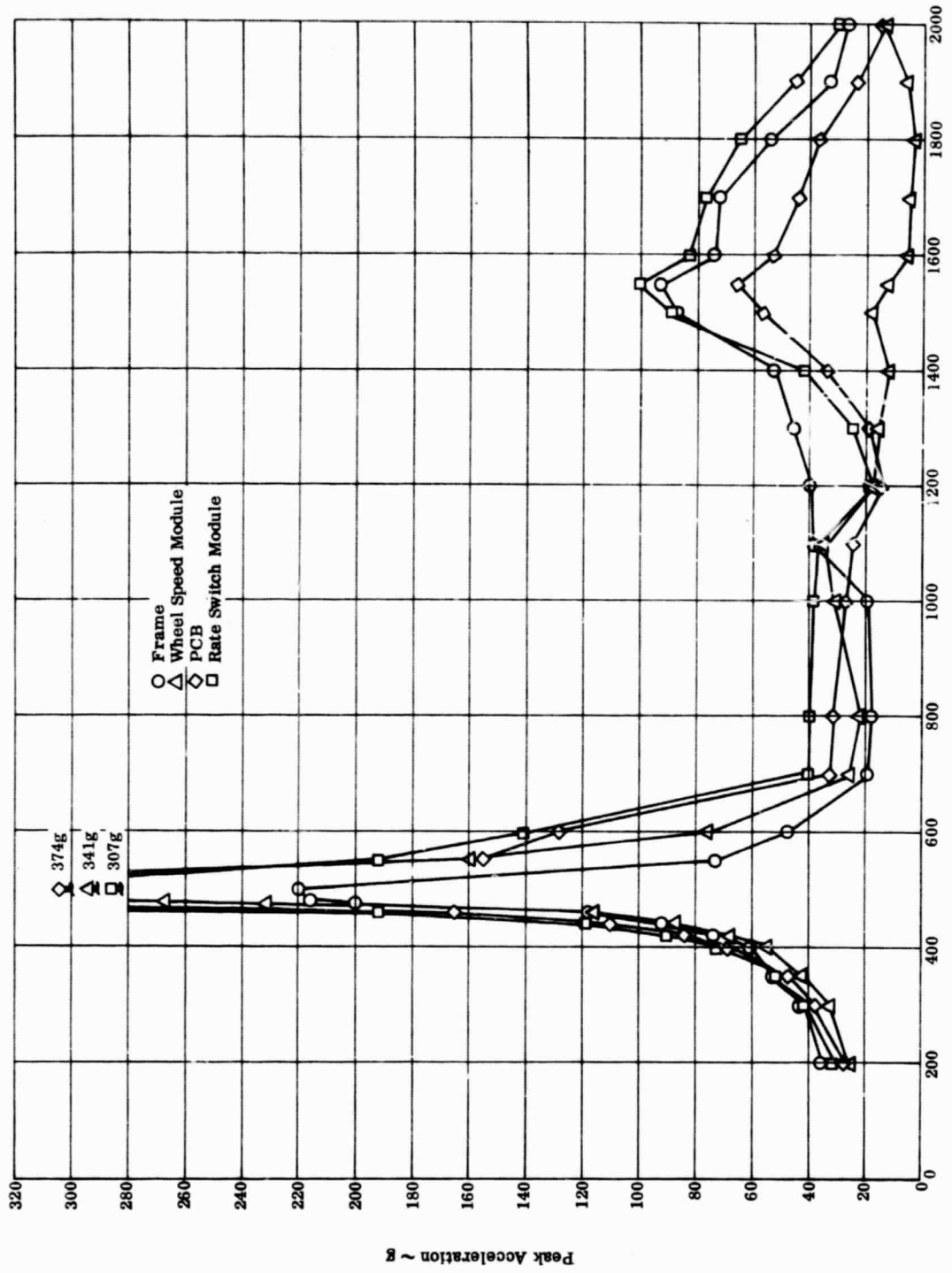


Figure 45. ACSP X Axis, PCB with RTV

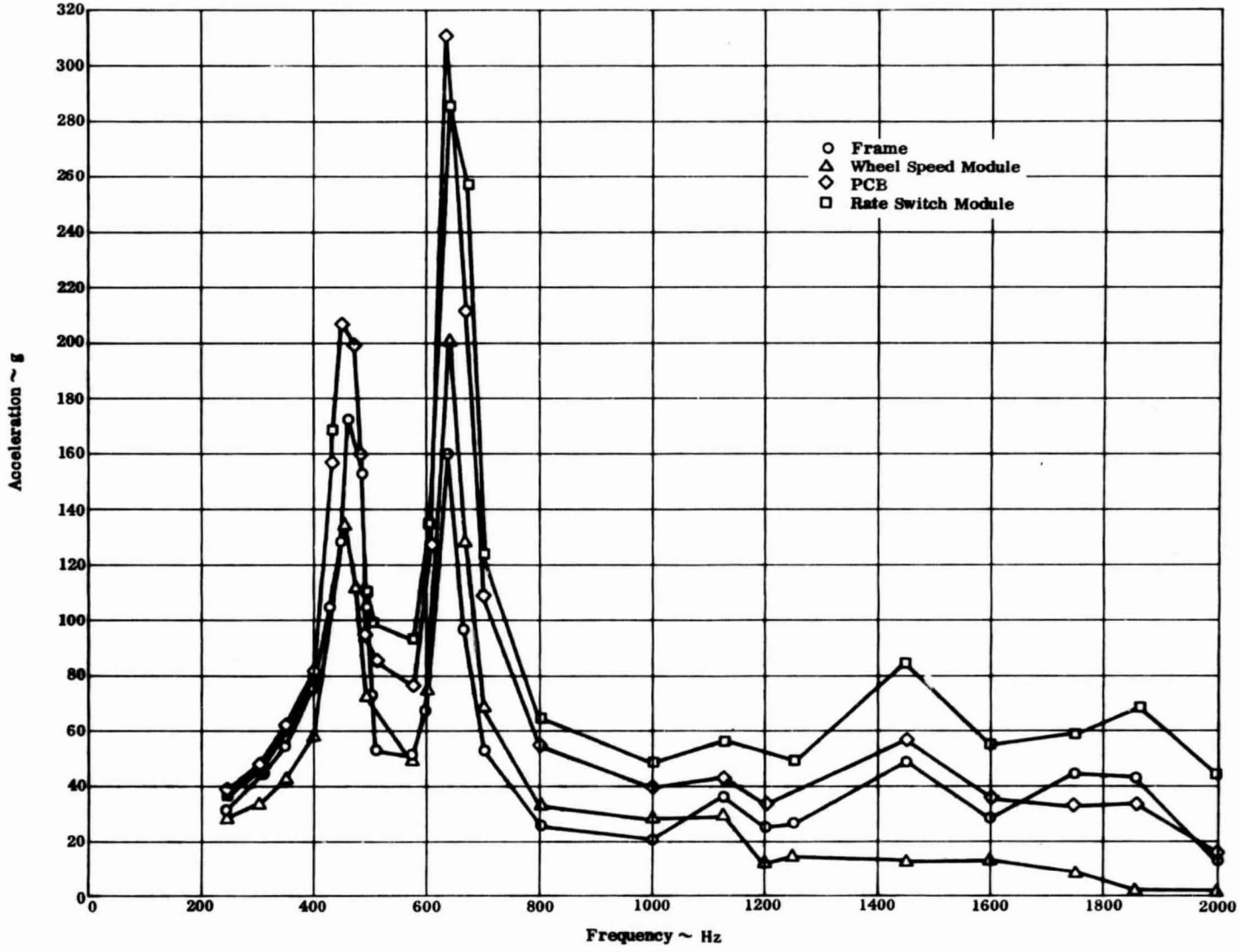


Figure 46. ACSP X Axis, PCB with Epoxy

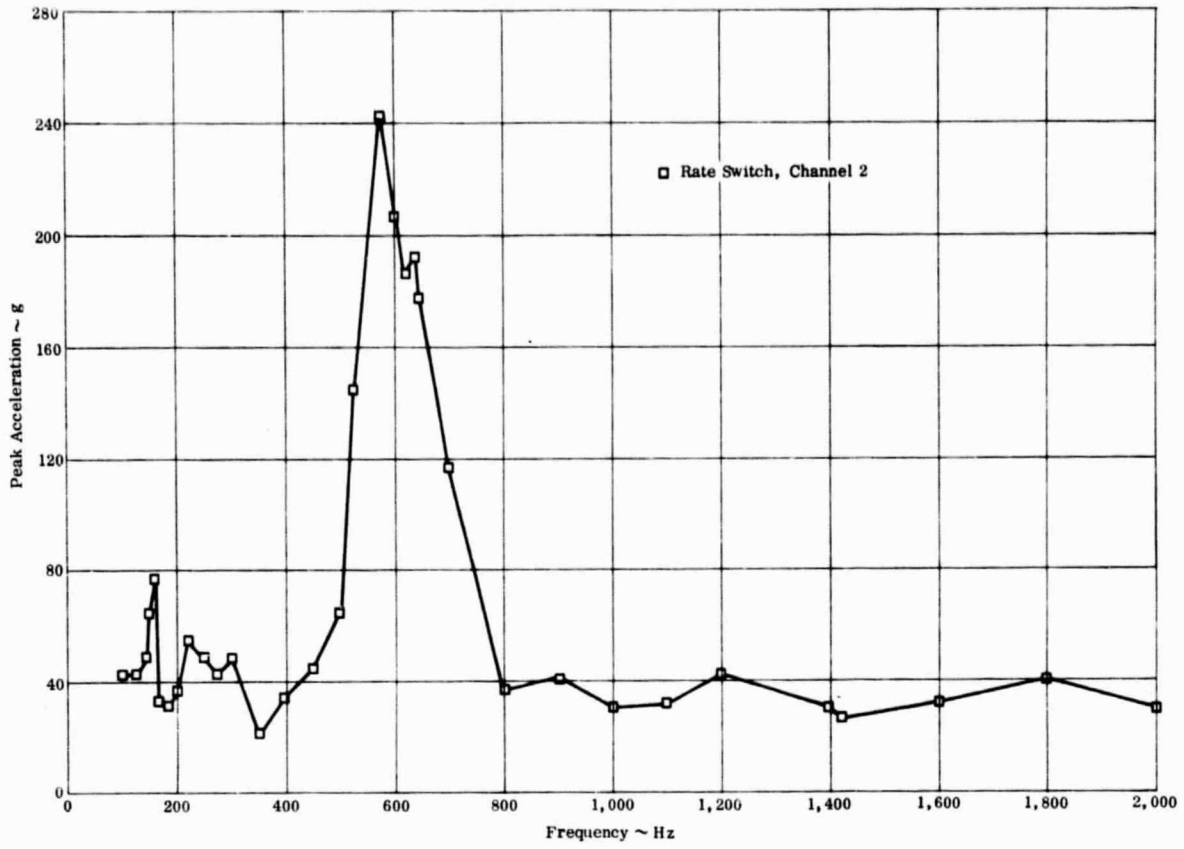


Figure 47. ACSP Dynamic Response, X Axis

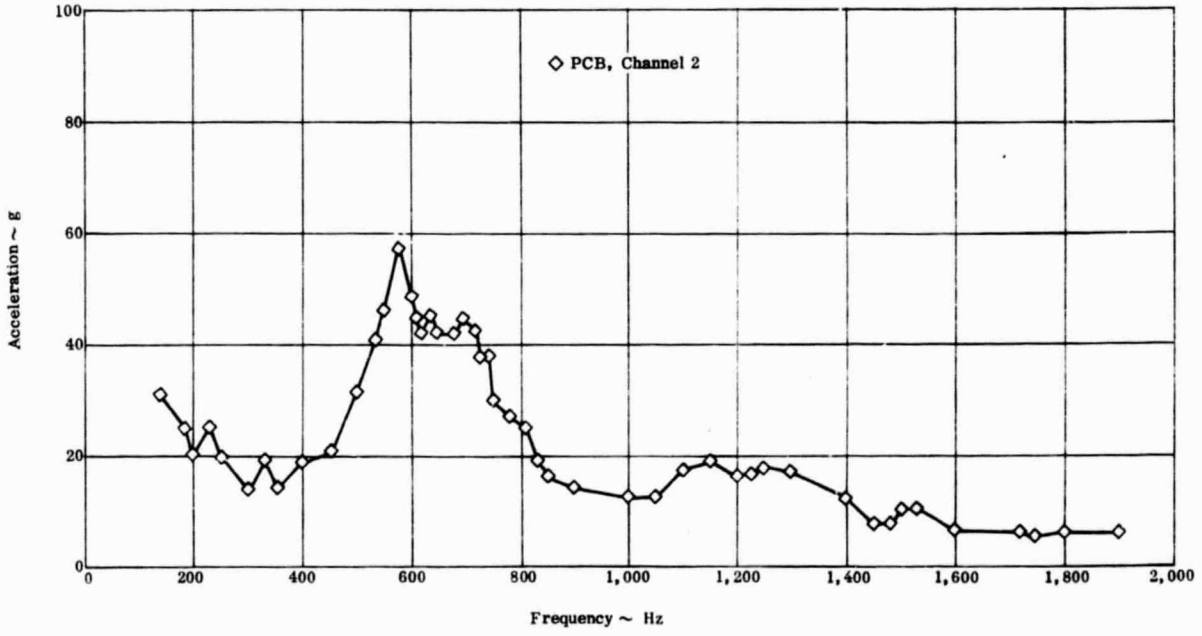


Figure 48. ACSP Dynamic Response, Y Axis

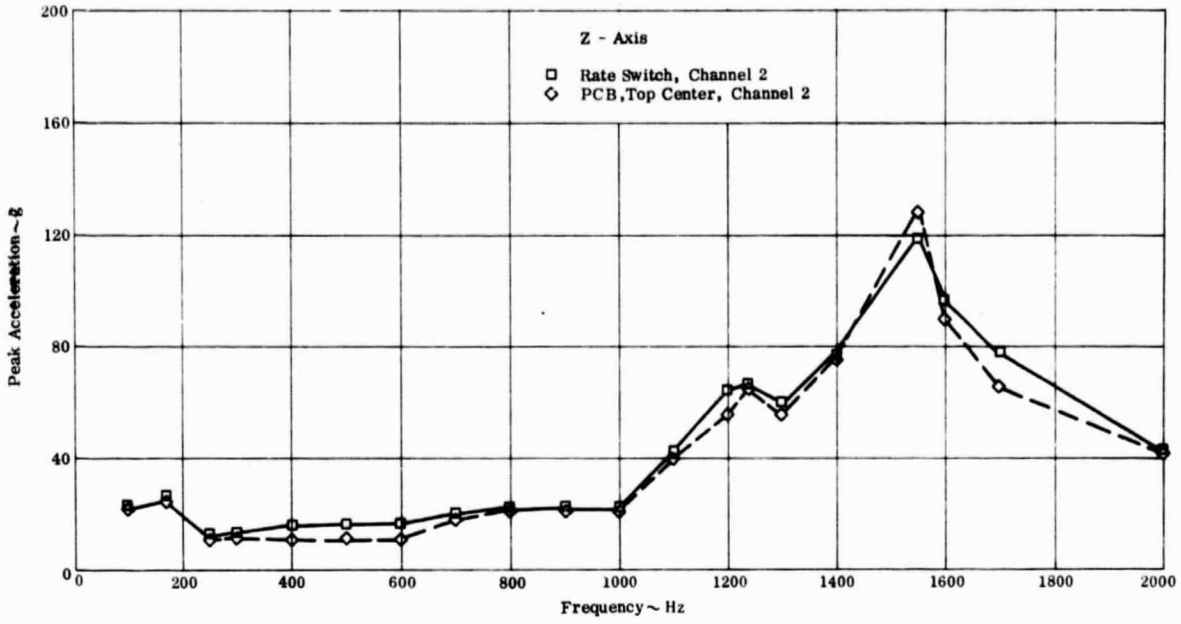


Figure 49. ACSP Dynamic Response, Z Axis

TABLE XII

Relative Pin Displacements (Z-axis)

Configuration	Frequency (Hz)	PCB Displacement (inch)	Rate Switch Module Displacement (inch)	Wheel Speed Module Displacement (inch)	Maximum Relative Displacement (inch)
Plain PCB	630	0.0009	-	0.0013	0.0004
	1,070	0.0008	-	0.0005	0.0003
	1,750	0.0005	-	0.0003	0.0002
Epoxy PCB	600	0.0010	0.0013	0.0008	0.0003
	720	0.0008	0.0008	0.0005	0.0003
	1,000	0.0006	0.0008	0.0005	0.0002
	1,300	0.0003	0.0004	0.0003	0.0001
RTV PCB	600	0.0010	0.0008	0.0006	0.0004
	900	0.0004	0.0003	0.0002	0.0002
	1,130	0.0003	0.0005	0.0003	0.0002
	1,700	0.0003	0.0001	0.0002	0.0002
	1,800	0.0006	0.0002	0.0003	0.0004

Note: Frequencies selected were those felt to be most meaningful to evaluation of the pin deflection.

At this point in the development program, all problem areas contributing to vibration response within the ACSP structure had been resolved with the exception of the apparent high acceleration levels. This was not considered to be a problem area since the critical parts and subassembly interfaces within the box were performing within specifications. The one exception to this conclusion was the module. As previously stated, parts quality and processing problems would, of necessity, have to be resolved before internal responses and the module fragility levels could be considered compatible.

4. Qualification Vibration Testing

Final vibration tests on the ACSP were performed with all development modification incorporated. The vibration input levels are shown in Figures 50 and 51. The ACSP performed as expected in the sinusoidal evaluations. "A" modules were removed at the sign of malfunction, replaced, and the test continued. Four malfunctions were attributed to faulty component parts within the modules. In the random evaluations, only one module failure was observed. Although the original test durations were reduced for these runs, the maximum acceleration amplitudes were retained. The gain in overall performance is attributed basically to the improvements achieved during developmental efforts and the module screening.

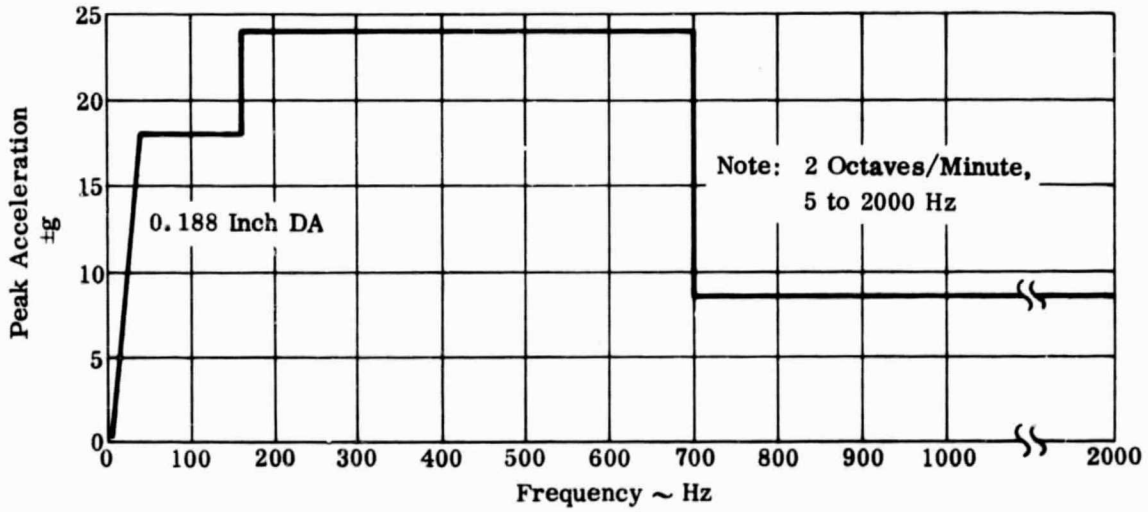
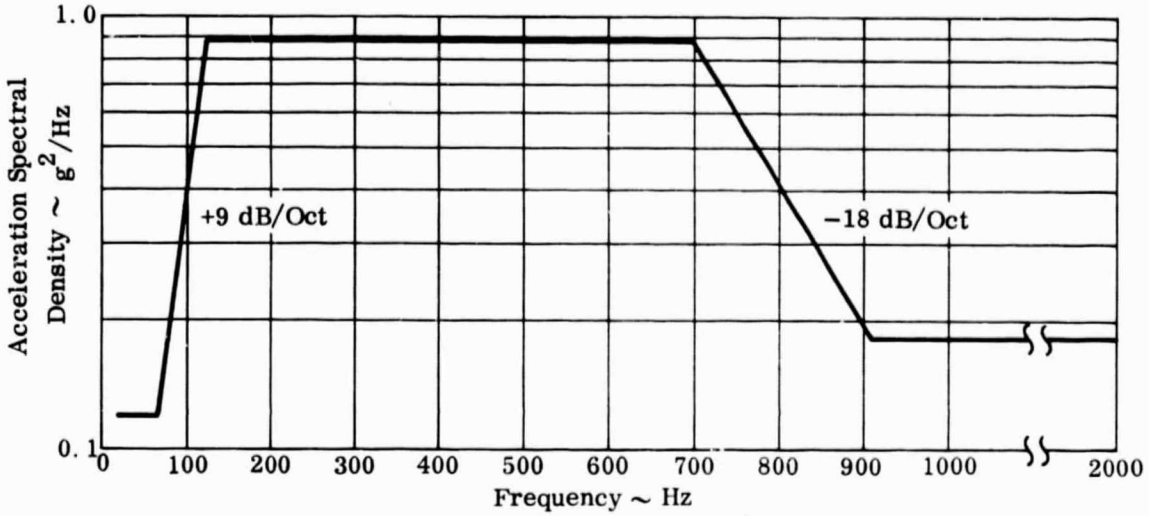


Figure 50. Sine Qualification Test



Note: Y Axis - 1 1/2 min at 20g rms, 1 1/2 min at 30g rms
X Axis - 1/2 min at 20g rms, 1/2 min at 30g rms
Z Axis - 1/2 min at 20g rms, 1/2 min at 30g rms

Figure 51. Random Qualification Test

5. Qualification Shock Testing

These tests were run on a Hyge Shock Actuator in accordance with the requirements of Table VIII. The ACSP was operating before, during, and after the shock transient. No malfunctions or physical failures were observed during the test or in the post-test inspection. Figure 52 shows the ACSP mounted on the shock test machine. Figure 53 shows the controlled input to the ACSP mounting base for each of the test runs.

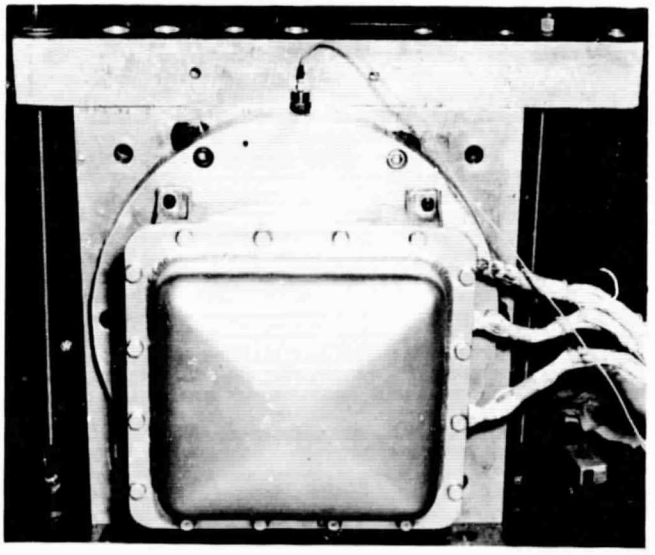


Figure 52. ACSP Shock Test

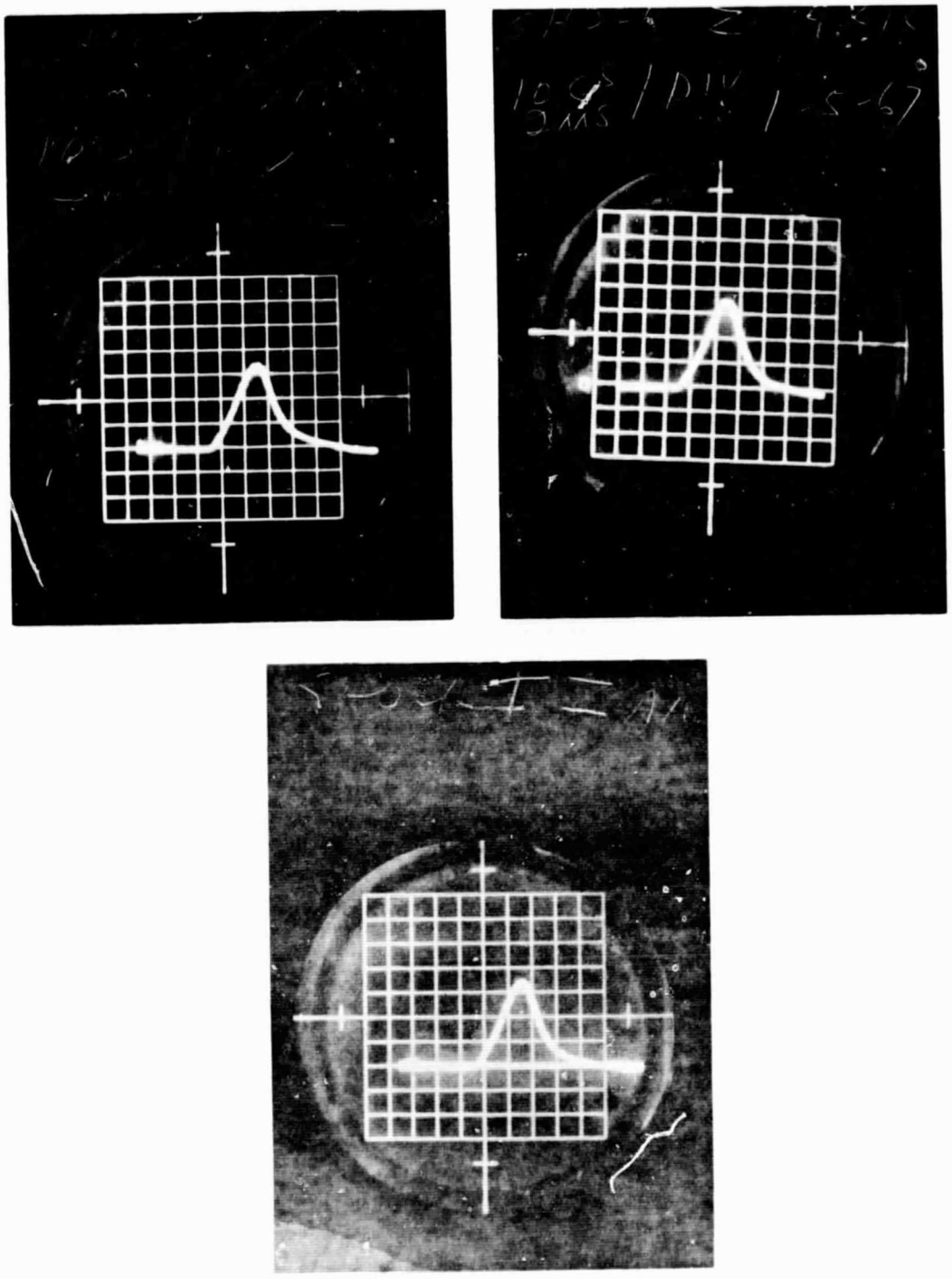


Figure 53. ACSP Shock Test Input Pulses

6. Qualification Acceleration Testing

The steady acceleration tests were performed on a Shavitz centrifuge in accordance with the requirements of Table VIII. The ACSP operated properly during and after the applied steady acceleration in each of the runs. Post-test inspection revealed no physical deformation or structural failures. Figure 54 shows the ACSP mounted on the centrifuge for one of the runs.

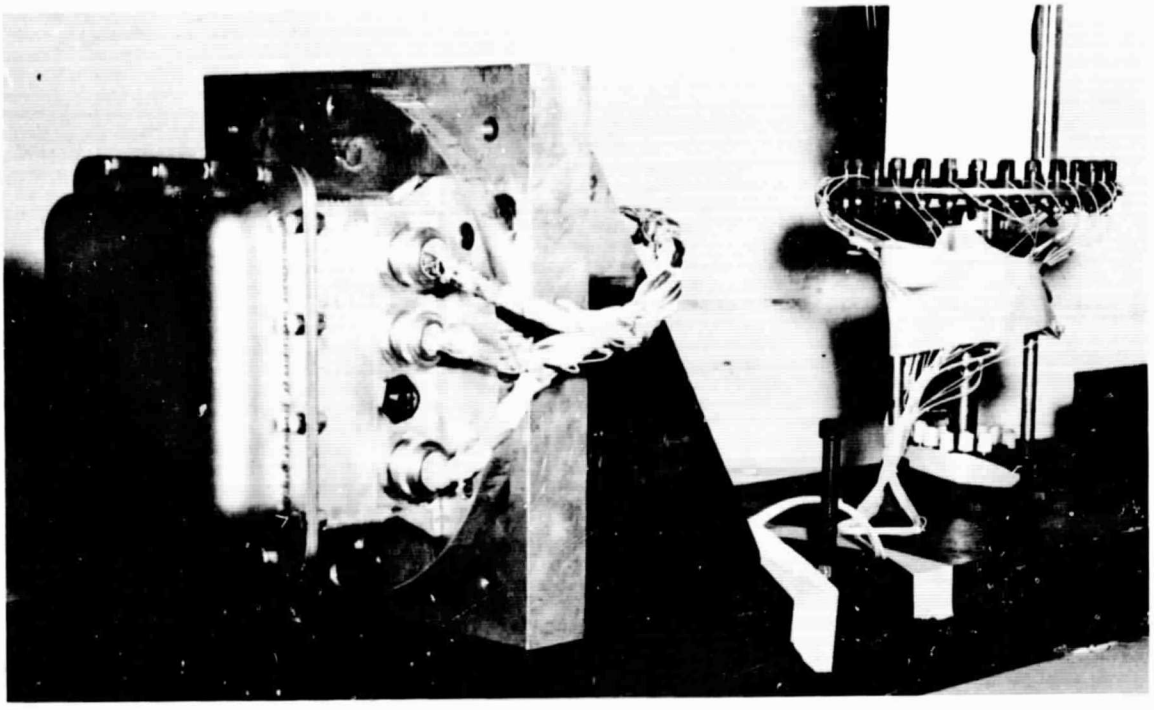


Figure 54. ACSP Acceleration Test